STIC Search

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SYSTEM:OS  - DIALOG OneSearch
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         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online 1861-2005/Mar
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         (c)2005 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs 1983-2005/Feb
         (c) 2005 The HW Wilson Co.
  File 144:Pascal 1973-2005/Mar W3
         (c) 2005 INIST/CNRS
  File 305:Analytical Abstracts 1980-2005/Mar W3
         (c) 2005 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs 1970-2005/Feb
         (c) 2005 DECHEMA
  File 350:Derwent WPIX 1963-2005/UD,UM &UP=200519
         (c) 2005  Thomson Derwent
*File 350: For more current information, include File 331 in your search.
Enter HELP NEWS 331 for details.
  File 347:JAPIO Nov 1976-2004/Nov(Updated 050309)
         (c) 2005 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs Aug 1985-2004/May
         (c) 2004 European Patent Office
  File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
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Set      Items    Description
S1         428    AU=(MANNA, I? OR MANNA I?)
S2        4159    AU=(LO, K? OR LO K?)
S3        2177    AU=(TAN, P? OR TAN P?)
S4         223    AU=(FILIPPI, R? OR FILIPPI R?)
S5        6970    S1:S4
S6          89    S5 AND (MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS?
               ? OR N()MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ?
                OR C()MOS? ? OR CMOS? ? OR NMOSFET? ? OR NMOS()FET? ? OR PMO-
               S()FET? ? OR PMOSFET? ?)
S7          47    S6 AND (DMOS()FET? ? OR DMOSFET? ? OR UMOS()FET? ? OR UMOS-
               FET? ? OR MOS()FET? ? OR MOSFET? ?)
S8           3    S7 AND (PIN OR "P"()(INTRINSIC? OR SEMICONDUCT?)()DIODE OR
               "P"()"N " OR "P"()"I"()"N" OR ("P" OR "N")(2N)REGION?)
S9          44    S7 NOT S8
S10          0    S9 AND GATE(2N)ELECTROD?
S11     469052    (MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS? ? OR N-
               ()MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ? OR C-
               ()MOS? ? OR CMOS? ? OR NMOSFET? ? OR NMOS()FET? ? OR PMOS()FE-
               T? ? OR PMOSFET? ?)
S12     122377    DMOS()FET? ? OR DMOSFET? ? OR UMOS()FET? ? OR UMOSFET? ? OR
                MOS()FET? ? OR MOSFET? ?
S13      89092    CC=(B2560R OR B2560S) OR MC=S01-G02B OR IC=(G01R-031/26 OR
               G01R-031/27)
S14     590867    S11:S13
S15     599759    PIN OR "P"()(INTRINSIC? OR SEMICONDUCT?)()DIODE OR "P"()"N
               " OR "P"()"I"()"N" OR ("P" OR "N")(2N)REGION?
S16       4148    (LATERAL? OR HORIZONTAL?)(2N)(PIN OR "P"()(INTRINSIC? OR S-
               EMICONDUCT?)()DIODE OR "P"()"N " OR "P"()"I"()"N" OR ("P" OR -
               "N")(2N)REGION?)
S17     599759    S15:S16
S18      91997    GATE??(2N)ELECTROD?
S19      95083    TRANSIST?(2N)(DIODE OR GATE?? OR ELECTROD?)
S20       4939    DIODE(2N)(GATE??()ELECTROD? OR GATE?? OR ELECTROD?)
S21      13693    DIODE(2N)(P()N OR P()I()N OR PIN OR P()INTRINSIC?)
S22     112546    S19:S21
S23      26330    S14 AND S17
S24       4720    S23 AND S18
S25        578    S24 AND S22
S26          4    S25 AND S16
S27          4    RD (unique items)
S28        574    S25 NOT S26
S29        574    S28 AND S15
S30        126    S29 AND S12
S31         13    S30 AND S21
S32         13    RD (unique items)
S33        113    S30 NOT S31
S34         11    S33 AND S20
S35         11    RD (unique items)
S36        102    S33 NOT S34
S37        102    S36 AND S19
S38         71    S37 AND S11
S39          2    S38 AND S13
S40          2    RD (unique items)
S41         90    S16 AND S12
S42          5    S41 AND S21
S43          4    RD (unique items)
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S44          4    S43 NOT S31,S34,S39
S45         29    S18 AND S16
S46          8    S45 AND S12
S47          8    RD (unique items)
S48          8    S47 NOT S31,S34,S39,S43
S49         21    S45 NOT S46
S50         17    RD (unique items)
S51          0    S50 AND S20
S52          5    S50 AND S19
S53         12    S50 NOT S52
S54          9    S53 AND S11
S55          3    S53 NOT S54
```

8/3,AB/1 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2005 Inst for Sci Info. All rts. reserv.

04237790 Genuine Article#: RQ561 Number of References: 18
Title: SIMULATION, FABRICATION AND CHARACTERIZATION OF A NOVEL **P-I-N**-DRAIN **MOSFET** STRUCTURE FOR HOT-CARRIER SUPPRESSION (Abstract Available)
Author(s): JUNG LT; **MANNA I**; BANERJEE SK
Corporate Source: UNIV TEXAS,MICROELECTR RES CTR/AUSTIN//TX/78712
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1995, V42, N9 (SEP), P 1591-1599
ISSN: 0018-9383
Language: ENGLISH Document Type: ARTICLE
Abstract: A new **P-I-N**-drain **MOSFET** structure has been developed with;very low (near-intrinsic) doping (10(15)-10(16) Cm-3 in our case) in the channel near the source/drain ends. The new structure is more effective in reducing the peak electric field at the channel/drain junction than LDD structures, and hence results in better hot carrier suppression. Also, simulations show that the near-intrinsic region near the drain reduces the transverse electric field and gives rise to higher carrier mobility and drive current. Experimental results show that, with the new structure, the substrate current and oxide charging due to hot-carrier injection are greatly reduced.

8/3,AB/2 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2005 INIST/CNRS. All rts. reserv.

12275003 PASCAL No.: 95-0505538
Simulation, fabrication and characterization of a novel **P-I-N**-drain **MOSFET** structure for hot carrier suppression
JUNG L T; **MANNA I**; BANERJEE S K
Univ of Texas, Austin TX, USA
Journal: IEEE Transactions on Electron Devices, 1995, 42 (9) 1591-1599
Language: English
A new **P-I-N**-drain **MOSFET** structure has been developed with very low (near-intrinsic) doping (10 SUP 1 SUP 5 -10 SUP 1 SUP 6 cm SUP - SUP 3 in our case) in the channel near the source/drain ends. The new structure is more effective in reducing the peak electric field at the channel/drain junction than LDD structures, and hence results in better hot carrier suppression. Also, simulations show that the near-intrinsic region near the drain reduces the transverse electric field and gives rise to higher carrier mobility and drive current. Experimental results show that, with the new structure, the substrate current and oxide charging due to hot-carrier injection are greatly reduced.

8/3,AB/3 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2005 INIST/CNRS. All rts. reserv.

11466307 PASCAL No.: 94-0303297
New **pin MOSFET** structure for hot carrier suppression
**MANNA I**; JUNG L; BHATTACHARYA S; BANERJEE S
Univ. Texas, microelectronics res. cent., Austin TX 78705, USA
Journal: Electronics letters, 1994, 30 (5) 457-459
Language: English
As an alternative to lightly doped drain (LDD) structures, a new

**pin MOSFET** structure has been developed with near-intrinsic doping in the channel near the source/drain ends. This new structure has better hot carrier suppression, current drive capability and short channel effects compared to LDD **MOSFETs**

27/3,AB/1     (Item 1 from file: 2)
DIALOG(R)File   2:INSPEC
(c) 2005 Institution of Electrical Engineers. All rts. reserv.

02078573   INSPEC Abstract Number: B83038927
Title: Submicron-gate self-aligned GaAs FET by ion implantation
Author(s): Matsumoto, K.; Hashizume, N.; Atoda, N.; Tomizawa, K.; Kurosu, T.; Iida, M.
Author Affiliation: Electrotech. Lab., Ibaraki, Japan
Conference Title: Gallium Arsenide and Related Compounds, 1982. Tenth International Symposium on Gallium Arsenide and Related Compounds p. 317-24
Editor(s): Stillman, G.E.
Publisher: IOP, Bristol, UK
Publication Date: 1983  Country of Publication: UK    xvi+650 pp.
ISBN: 0 85498 156 X
U.S. Copyright Clearance Center Code: 0305-2346/83/0065-0317$02.25
Conference Sponsor: Air Force Office Sci. Res
Conference Date: 19-22 Sept. 1982    Conference Location: Albuquerque, NM, USA
Language: English

Abstract: A self-aligned GaAs FET employing a tungsten metal as the **gate electrode** and at the same time as a mask for the ion implantation for the **n/sup +/-regions** is reported. The transconductance of 255 mS/mm was observed with a 0.8 mu m-gate FET. It was found that the implanted Se ions in the **n/sup +/-regions** diffuse **laterally** into the active region during the annealing. Dependence of the FET characteristics on the gate length, annealing time, and crystal orientation is investigated.

Subfile: B

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27/3,AB/2     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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008060633
WPI Acc No: 1989-325745/198945
XRPX Acc No: N89-248001

Switchable power semiconductor with insulated **gate** bipolar **transistors** - has unit cells associated with **MOS** controlled thyristors turned-off by field-effect-controlled short-circuit

Patent Assignee: ASEA BROWN BOVERI AG (ALLM  ); ASEA BROWN BOVERI A (ALLM  )
Inventor: BAUER F
Number of Countries: 012  Number of Patents: 005
Patent Family:

```
Patent No     Kind   Date     Applicat No    Kind   Date      Week
EP 340445      A   19891108  EP 89105333     A   19890325  198945  B
JP 2012969     A   19900117  JP 8999898      A   19890419  199009
US 4967244     A   19901030  US 89334967     A   19890407  199046
EP 340445      B1  19930825  EP 89105333     A   19890325  199334
DE 58905355    G   19930930  DE 505355       A   19890325  199340
                             EP 89105333     A   19890325
```

Priority Applications (No Type Date): CH 881520 A 19880422
Patent Details:

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Patent No  Kind Lan Pg   Main IPC    Filing Notes
EP 340445     A  G   7
   Designated States (Regional): AT BE CH DE FR GB IT LI NL SE
```

EP 340445 B1 G 8 H01L-029/74
Designated States (Regional): AT BE CH DE FR GB IT LI NL SE
DE 58905355 G H01L-029/74 Based on patent EP 340445

Abstract (Basic): EP 340445 A

The **MOS** contro-led thyristor (MCT) responsible for the turn-off process is associated with an insulated **gate** bipolar **transistor** (IGBT) whose p-type emitter layer (9) and n-type base layer (8) are of continuous form. The heavily-doped **p**-type **region** (13) is bounded **laterally** by **p**-doped channel **regions** (12) and inlaid **n**+ doped source **regions** (11), which with the n-type base layer (12) form an n-channel **MOSFET**.

The IGBT unit cell guarantees the turn-off of the thyristor. **Gate electrodes** (3) are held pref. at the same potential so that adjacent MCT and IGBT unit cells are controlled by the same gate.

ADVANTAGE - Can be optimised easily with regard to channel length, and affords more flexibility in respect of layout of component.

3/3

Abstract (Equivalent): EP 340445 B

Power semiconductor component with turn-off facility in which (a) next to each other and connected in parallel in a semiconductor substrate (14) between an anode (A) and a cathode (K); (b) each of said first unit cells is constructed as an **MOS**-controlled thyristor (MCT = **MOS** Controlled Thyristor) which can be turned off by means of a field-effect-controlled short circuit; (c) each of the first unit cells comprises, between the anode and the cathode a layer sequence composed of a p+ -doped p-type emitter layer, an n-doped n-type base layer, a p-doped p-type base layer (7) and an n+-doped **n**-type emitter **region** (6) with **laterally** adjacent **n**-doped channel **regions** (5) and embedded **p**+-doped source **regions** (4); (d) in each of the first unit cells, the source regions, the channel **regions** and the **p**-type base layer emerge next to each other at the cathode-side surface of the semiconductor substrate and in each case form an n-channel **MOSFET** with an insulated **gate electrode** (3) situated above it; and (e) additional means are provided which ensure the field effect controlled turning-on of the component; characterised in that (f) the additional means comprise second unit cells which, independently of the first unit cells, are arranged between the latter and are connected in parallel with the latter; (g) each of the second unit cells has the structure of a bipolar **transistor** with insulated **gate** (IGBT = Insulated **Gate** Bipolar **Transistor**), in which (h) each of the second unit cells comprises, between the anode and the cathode, a layer sequence composed of a p+ -doped p-type emitter layer, an n-doped n-type base layer, and a p+ -doped **p**-type **region** (13), embedded in the n-type base layer, with **laterally** adjacent **p**-doped channel **regions** (12) and embedded **n**+-doped source **regions** (11); (i) in each of the second unit cells, the source regions, the channel regions (1) and the n-type base layer emerge next to each other at the cathode-side surface of the semiconductor substrate and in each case form an n-channel **MOSFET** with an insulated **gate electrode** situated above it; (k) the source **regions** and the **p**+-type **region** are connected directly to the cathode via a cathode contact; and (i) the p-type emitter layers and the n-type base layers of both unit cells are in each case part of a common p-type emitter layer (9) or n-type base layer (8) respectively extending laterally over the semiconductor substrate.

(Dwg.1/3

Abstract (Equivalent): US 4967244 A

The component consists of a number of unit cells arranged parallel to each other. Each cell is a **MOS**- controlled thyristor (MCT) which can be switched off by a field-effect-controlled short circuit. Bipolar-**transistor**-with-insulated-**gate** (IGBT) cells connected in parallel with the MCT unit cells ensure switching on.

Each MCT unit cell has a sequence of heavily doped emitter and medium doped base layers of different conducting types forming a first conductivity-type-channel **MOSFET** with an insulated **gate electrode** above it. The IGBT unit cells form a second conductivity type-channel **MOSFET** with an insulated **gate electrode** above it. The p-type emitter layers and the n-type base layers of both elementary cells are in each part of a commen p-type emitter layer or n-type base layer respectively extending laterally over the semi-conducted substrate.

ADVANTAGE - Improved switch-on capability and increased flexibility in designing component

27/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004131865
WPI Acc No: 1984-277405/198445
XRAM Acc No: C84-117583
XRPX Acc No: N84-207067

Semiconductor ROM device - includes poly-silicon conductive layer which contacts **MOS** transistor memory cell drains and lies near and on **gate electrode**

Patent Assignee: TOSHIBA KK (TOKE )
Inventor: ARIIZUMI S; IWASE T; MASUOKA F
Number of Countries: 006 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 124115 | A | 19841107 | EP 84104787 | A | 19840427 | 198445 | B |
| JP 59201461 | A | 19841115 | JP 8375026 | A | 19830428 | 198501 | |
| US 4737835 | A | 19880412 | US 86919556 | A | 19861016 | 198817 | |
| US 4855248 | A | 19890808 | US 88143068 | A | 19880112 | 198939 | |
| EP 124115 | B | 19901024 | | | | 199043 | |
| DE 3483437 | G | 19901129 | | | | 199049 | |

Priority Applications (No Type Date): JP 8375026 A 19830428
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 124115 | A | E | 20 | | |

Designated States (Regional): DE FR GB IT

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 124115 | B | | | | |

Designated States (Regional): DE FR GB IT

Abstract (Basic): EP 124115 A

Read only memory semiconductor device comprises: **n+ regions** (12,13) formed in p substrate (11) forming drain and source of a **MOS transistor**; **gate** insulation film (21); **gate electrode** (14); **gate** insulation (22,23); n+ conductive layer (16) formed on one of the **n+ regions** and extending onto the gate insulation film (22,23); and third conductive layer (18) formed on n+ conductive layer (16).

Device is made by: forming **p** field insulation **region** in substrate (11); forming gate insulation (21); forming **gate electrode** (14); doping n impurity to form **n regions**

(12,13); depositing insulating film (22); forming contact hole (15), forming patterned n conductive layer (16); forming insulating film (24) with contact hole (17); and forming patterned conductive layer (18). Layer (16) is pref. a CVD polySi layer which is either pre-doped or implanted.

USE - In contact method data writing. Device has a small memory cell area and high integration density.

4/6

Abstract (Equivalent): EP 124115 B

1. A semiconductor read only memory device comprising:

a pair of regions (12,13) of a first conductivity type formed in a semiconductor substrate (11) of a second conductivity type opposite to said first conductivity type, the pair of regions individually forming drain and source regions of a **MOS** transistor; a first insulation film (21) for gate insulation formed on said substrate; a first conductive layer (14) for a **gate electrode** (140) formed on said gate insulation film; a second insulation film (22,23) formed on said **gate electrode**; a second conductive layer (16) containing an impurity of said first conductivity formed to contact one of said pair of regions, the second conductive layer extending onto said second insulation film (22,23) which is on said **gate electrode**; a third insulation film (24) having a contact hole leading to said second conductive layer (16); and a third conductive layer (18) formed to establish contact with said second conductive layer via said contact hole of said third insulation film (24), characterised in that: said contact hole of the third insulation film is above a portion of said one of said pair of regions and an adjacent portion of said **gate electrode**; and said third conductivity layer (18) extends to said second conductive layer via said contact hole of said third insulation film, so that the third conductive layer contacts said second conductive layer above said one of the pair of regions and said **gate electrode**.

(12pp

Abstract (Equivalent): US 4737835 A

Read only memory semiconductor device consists of matrix of memory cells (10), with **n+ regions** (12) formed in the **region** of a **P**-type semiconductor substrate (11), while a **laterally** extending **N+ region** (13) forms a common source for the cells in a row. **Gate electrodes** (14) extend between source and drain (12, 13) of each cell in a row. Drain regions are in contact with a second conductive layer (16) extending as common gate over the word line (14) or a first interconnection layer through contact holes (15). Data lines (18) are formed for each column while contacting memory cells for data to be written through contact holes (17). Field oxidn. film (20) separates elements and gate insulation (21) lies under the word line (14). Further oxidn. films (22-24) are incorporated and a layer (25) under field oxidn. film (20) prevents formation of a parasitic inversion layer.

ADVANTAGE - Memory cells occupy small area using contact method for data writing.

(9pp

27/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

01598954
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-077454 [JP 60077454 A]
PUBLISHED: May 02, 1985 (19850502)
INVENTOR(s): SHINOHARA MAMORU
TSUBONE HITOSHI
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-184520 [JP 83184520]
FILED: October 04, 1983 (19831004)
JOURNAL: Section: E, Section No. 340, Vol. 09, No. 216, Pg. 127, September 03, 1985 (19850903)

## ABSTRACT

PURPOSE: To enable to control the gain of a lateral transistor by implanting the same ions on the bases of lateral transistor simultaneously when implanting P type impurity ions on the gate of an insulated **gate** type **MOS** **transistor** for controlling the threshold voltage of the transistor when providing a **P**-**N**-P type **lateral** transistor and the **MOS** transistor on the same semiconductor substrate.

CONSTITUTION: An N type layer 3 is epitaxially grown on a P type Si substrate 1, the layer 3 is separated via an separating region 2 into two islands, one of which is used as a **P**-**N**-P type **lateral** bipolar transistor forming region and the other of which is used as an insulated **gate** type **MOS** **transistor** forming region. Then, to control the threshold voltage of the **MOS** transistor, B(sup +) ions are implanted to the gate to form a layer 9. Then, the ions are simultaneously implanted also to the base of the bipolar transistor. Thereafter, diffused regions 4, 5 are formed in normal way, and a **gate** **electrode** 7 made of polycrystalline Si is mounted on the **MOS** transistor.

32/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011833525
WPI Acc No: 1998-250435/199822
Related WPI Acc No: 1999-394670
XRAM Acc No: C98-078012
XRPX Acc No: N98-197750
Highly sensitive photo sensor structure - for enlarging the detected photo current from a **PIN** photo **diode** by a **MOSFET**
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: LIN C H
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5739065 | A | 19980414 | US 95542696 | A | 19951013 | 199822 | B |

Priority Applications (No Type Date): US 95542696 A 19951013
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5739065 | A | | 5 | H01L-021/82 | |

Abstract (Basic): US 5739065 A

Fabricating a sensitive photo sensor comprises: forming a well region in a substrate; sequentially depositing on the well region a gate oxide layer, a P-type polysilicon layer, an intrinsic type amorphous silicon layer, an N-type amorphous silicon layer, a transparent conducting layer; forming a gate photoresist on the transparent conducting layer; forming a gate by etching the conductive layer, the N-type silicon layer, the intrinsic type amorphous silicon layer and the P-type polysilicon layer using the gate photoresist as a mask, and then removing the gate photoresist; implanting heavily doped impurity into the substrate using the gate as a mask to form source and drain regions; depositing a dielectric layer on the gate, and the source and drain regions; forming gate sidewall spacers beside the gate by etching the dielectric layer; forming **electrodes** of the **gate**, and the source and drain regions.

USE - Structure for a highly sensitive photo sensor allocated in a **MOS** element.

ADVANTAGE - High sensitivity photo sensor, i.e. a **PIN** photo **diode** is allocated in a **MOSFET** thus enlarging the detected small photo current from the **PIN** photo **diode**.

Dwg.6/6

32/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009197493
WPI Acc No: 1992-324925/199240
XRPX Acc No: N92-248380
Insulated **gate** bipolar junction **transistor** with over voltage protection - has integrated clamping transistor and associated **P-N diode** that by-pass main **transistor gate**
Patent Assignee: FUJI ELECTRIC CO LTD (FJIE ); FUJI ELECTRIC MFG CO LTD (FJIE )
Inventor: SAKURAI K
Number of Countries: 003 Number of Patents: 004

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| DE 4208695 | A | 19920924 | DE 4208695 | A | 19920318 | 199240 | B |
| JP 4291767 | A | 19921015 | JP 9155202 | A | 19910320 | 199248 | |
| US 5221850 | A | 19930622 | US 92819793 | A | 19920113 | 199326 | |
| DE 4208695 | C2 | 20001207 | DE 4208695 | A | 19920318 | 200064 | |

Priority Applications (No Type Date): JP 9155202 A 19910320

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| DE 4208695 | A | | 10 | H01L-029/784 | |
| JP 4291767 | A | | 6 | H01L-029/784 | |
| US 5221850 | A | | 9 | H01L-029/06 | |
| DE 4208695 | C2 | | | H01L-029/78 | |

Abstract (Basic): DE 4208695 A

The main insulated **gate** bipolar junction **transistor** (IGBT) is formed from a substrate of one doping type (1), separated by a buffer layer (2) from a high resistance layer of a second doping type (3) diffused with a region of the first doping type (4,5) that forms the base of the **transistor**. A **gate electrode** (8) is sandwiched between two insulating layers (10,13) that insulate the electrode from the high resistance layer and the emitter contact (14) and associated emitter zones (7).

To protect against overvoltage conditions, a clamping transistor (24) is formed by diffusing a second region (6) of the first doping type into the high resistance layer to a deeper level (d2) than the main transistor level (d1), thereby forming second junction with a lower turn-on voltage than the main transistor. The clamping transistor is connected to the collector junction and the gate contacts of the main transistor by the high resistance layer and by a metallic layer (16) and a pn junction diode (25), the latter being formed by two small regions of different doping types (11,12).

ADVANTAGE - Integral clamping **transistor** and **diode** improve IGBT overvoltage protection.

Dwg.1/5

Abstract (Equivalent): US 5221850 A

A collector layer is formed of first conductivity type, with a high resistivity layer formed of second conductivity type and situated near the collector layer. A base region is formed selectively in a surface area of the high resistivity layer formed of the second conductivity type. An emitter region is formed selectively in a surface area of the base region and formed of the second conductivity type to form a channel region at an area between the high resistivity layer formed of the second conductivity type near the base region and the emitter region. A **gate electrode** is provided with an insulating film and is disposed on the channel region through the insulating film, with an emitter electrode connected to both the base region and the emitter region.

A collector electrode contacts the collector layer, with an annex region formed of the first conductivity type, selectively located in the surface area of the high resistivity layer formed of the second conductivity type and situated away from the base region. A low resistivity layer is formed on the second conductivity type and interposed between the high resistivity layer and the collector layer. A diode is formed between the annex **electrode** and the **gate electrode**, having a layer formed of the first conductivity type at a side of the annex electrode.

ADVANTAGE - Provides an IGBT which allows the withstand voltage of each and every transistor to be set at an approximately definite value

of 50 V or 100 V less than the withstand voltage of protection diodes without selection.
Dwg.1/5

32/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008504516
WPI Acc No: 1991-008600/199102
XRPX Acc No: N91-006764

**MOS** bipolar power semiconductor circuit element - uses heavily doped recombination layer in middle of base region

Patent Assignee: ASEA BROWN BOVERI A (ALLM )
Inventor: BAUER F; STOCKMEIER T
Number of Countries: 008 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 405200 | A | 19910102 | EP 90110790 | A | 19900607 | 199102 | B |
| US 4985741 | A | 19910115 | US 90546911 | A | 19900614 | 199106 | |
| JP 3044969 | A | 19910226 | JP 90171311 | A | 19900628 | 199114 | |

Priority Applications (No Type Date): CH 892440 A 19890630
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 405200 | A | | | | |

Designated States (Regional): CH DE GB IT LI SE

Abstract (Basic): EP 405200 A

The circuit element comprises a semiconductor substrate (12) with an anode (A), cathode (K), emitter layer (8), and collector region (6) projecting into base layer (7), source region (5), channel (13) and **gate electrode** (3). In particular, a heavily doped recombination layer (10) exits in the middle of the base layer (7), and may open to allow passage of electrons between regions (7a,7b) of base layer (7).

Preferably, the upper base layer (7a) is only a few microns thick, and has the same doping concentration as the lower base layer. The openings in the recombination layer (10) should be rectangular in shape thus making the layer (10) mesh shaped.

ADVANTAGE - High Voltage operation. (9pp Dwg.No.2/5

Abstract (Equivalent): US 4985741 A

A recombination layer (10) which is doped with the same polarity as the base layer but more highly, is inserted, starting with the structure of an IGBT, into the base layer between anode (A) and cathode (K), which recombination layer divides the base layer into an upper and lower base layer (7a and 7b respectively).

The resultant structure forms a series circuit **MOSFET** (T) and **PIN diode** (D) which is free of latch up and provides the possibility of higher blocking voltages. (7pp)

32/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007571181
WPI Acc No: 1988-205113/198829
XRPX Acc No: N88-156524

Bidirectional output semiconductor field effect transistor - has **diode**, **P-N**-P transistor and resistor integrated into same chip containing lateral BOS FET to form solid-state relay circuit

Patent Assignee: INT RECTIFIER CORP (INRC )

Inventor: KINZER D M

Number of Countries: 001  Number of Patents: 001

Patent Family:

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Patent No     Kind   Date     Applicat No    Kind   Date     Week
US 4755697     A   19880705  US 85755858     A   19850717  198829  B
```

Priority Applications (No Type Date): US 85755858 A 19850717

Patent Details:

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Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 4755697    A     16
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Abstract (Basic): US 4755697 A

The high voltage bidirectional output semiconductor field effect transistor (**MOSFET**) is turned on from the electrical output of a photovoltaic stack which is energised from an LED. The **MOSFET** device consists of two lateral field effect transistors formed in an implanted **N**(-) **region** in a **P**(-) substrate. Two spaced drain regions feed inwardly toward a common **N**(+) source **region** separated from the drains by respective P type diffusions. The surface of these diffusions can be inverted by application of voltage to the suitably disposed **gate electrode**. The depletion field between channel and drain regions is well controlled over the surface of the device. The source contact remains close to the potential of the gate contact at all times so that the device can be used for high voltage switching of either polarity.

A **diode**, PNP **transistor** and resistor are integrated into the same chip containing the lateral **MOSFET** device to form a solid state relay circuit having characteristics similar to a reed relay. The diode defines a forward conduction path from a photovoltaic pile voltage source directly to the **MOSFET** gate so that the **MOSFET** gate capacitance can be quickly charged during turn-on. The PNP transistor is a high gain transistor coupled to the diode and to the input resistance of the circuit. The input impedance of the circuit is reduced by the gain of the transistor when the photovoltaic output voltage is turned off and its voltage drops to below the gate voltage by about 0.6 volt to turn on the transistor.

ADVANTAGE - Can switch either AC or DC voltages, has extremely small leakage current when in off state, low thermal offset voltage, generates no electromagnetic interference radiation when closed

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32/3,AB/5     (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

03748579

SEMICONDUCTOR DEVICE

```
PUB. NO.:      04-113679  [JP 4113679  A]
PUBLISHED:     April 15, 1992 (19920415)
INVENTOR(s):   SHINOHARA TOSHIAKI
APPLICANT(s):  NISSAN MOTOR CO LTD [000399] (A Japanese Company or
               Corporation), JP (Japan)
APPL. NO.:     02-232941  [JP 90232941]
FILED:         September 03, 1990 (19900903)
JOURNAL:       Section: E, Section No. 1243, Vol. 16, No. 360, Pg. 99,
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August 04, 1992 (19920804)

ABSTRACT

PURPOSE: To eliminate damage of a power source even if the power source is reversely connected and to obtain a semiconductor device having small internal resistance by connecting a normal OFF type switch element in series with a source region side in a **MOS** type semiconductor device, and conducting the element when the device is conducted.

CONSTITUTION: A vertical **MOSFET** is formed of an N-type semiconductor substrate 1 of a drain **region,** a **P**-type well 2 of a base **region,** an **N** (sup +) type high concentration region 3 of a source region, and a **gate electrode** 5. An **MOSFET** of a switch element is formed of an SOI thin film 7, high concentration SOI regions 8, 9, and a **gate electrode** 5, and the **MOSFET** of the element is connected in series with the source region side of the vertical **MOSFET** . In the case of reverse connection, when the electrode 5 is set to a low potential, the **MOSFET** of the element is interrupted, while when it is set to a high potential, the **MOSFET** of the element is conducted, but the forward current of a **P-N** junction **diode** has a negative temperature coefficient.

32/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03386357
SEMICONDUCTOR DEVICE

| | |
|---|---|
| PUB. NO.: | 03-049257 [JP 3049257 A] |
| PUBLISHED: | March 04, 1991 (19910304) |
| INVENTOR(s): | SHINOHARA TOSHIAKI |
| APPLICANT(s): | NISSAN MOTOR CO LTD [000399] (A Japanese Company or Corporation), JP (Japan) |
| APPL. NO.: | 01-185136 [JP 89185136] |
| FILED: | July 18, 1989 (19890718) |
| JOURNAL: | Section: E, Section No. 1067, Vol. 15, No. 187, Pg. 146, May 14, 1991 (19910514) |

ABSTRACT

PURPOSE: To incorporate a Zener diode of a large capacity into an LSI chip by controlling a reverse breakdown voltage of a power source Zener diode by upper diffusion of impurity on a substrate and contour control of a high concentration region of a bottom section of a well region.

CONSTITUTION: An N-epitaxial layer 14 which is doped with N-type impurity of high concentration is formed on an upper side of an N(sup +)-substrate 13. A **P**-well **region** 15 is formed on the substrate 13 through ion implantation such as B and thermal diffusion. A **P**(sup +)-**region** 16 and an **N**(sup +)-**region** 17 are further formed thereon. Then, a **gate electrode** 18 is formed on an upper side thereof. An **MOSFET** region 19 and a guard ring region 12 are formed in this way. An impurity profile of the region 15 and an upper diffusion profile from the N(sup +)-substrate 13 come into contact with each other to a degree more than to hide impurity profile of the N-epitaxial layer 14; as a result, a reverse breakdown voltage of a formed **p-n** junction **diode** is set at more than a regular operational voltage and smaller than a withstand voltage of a semiconductor element.

32/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

02991120
INTEGRATED CONVERTER

PUB. NO.: 01-288720 [JP 1288720 A]
PUBLISHED: November 21, 1989 (19891121)
INVENTOR(s): ISHIHARA TSUTOMU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-119832 [JP 88119832]
FILED: May 16, 1988 (19880516)
JOURNAL: Section: P, Section No. 1003, Vol. 14, No. 66, Pg. 90, February 07, 1990 (19900207)

ABSTRACT

PURPOSE: To enable **MOS** integration, by arranging a **p-n** junction **diode**, a **MOSFET** switch, a **MOS gate electrode**-inversion layer capacitance type capacitor and a **MOS** operational amplifier to form a circuit.

CONSTITUTION: **MOSFETs** 21 and 22 form a current mirror and a bias voltage is supplied from a bias circuit comprising **MOSFETs** 23-25 to drive diodes 11 and 12 by a constant current. A capacitor 31 samples an electric charge proportional to a voltage drop of the diode 12 to hold it and a capacitor 32 samples an electric charge proportional to a difference in voltage drop between the diodes 11 and 12 to hold it. An operational amplifier 30 and a capacitor 33 and up the charge held as sample by the capacitors 31 and 32 to sample and hold them. Then, a detection circuit containing piezoelectric resistance elements 1-4 is driven by an output voltage of the operational amplifier 30 held by the capacitor 33. The circuit thus arranged permits adaption thereof to a **MOS** integration.

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32/3,AB/8 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

02402947
SEMICONDUCTOR MEMORY DEVICE

PUB. NO.: 63-019847 [JP 63019847 A]
PUBLISHED: January 27, 1988 (19880127)
INVENTOR(s): SASAKI MASAYOSHI
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-163849 [JP 86163849]
FILED: July 14, 1986 (19860714)
JOURNAL: Section: E, Section No. 627, Vol. 12, No. 228, Pg. 20, June 28, 1988 (19880628)

ABSTRACT

PURPOSE: To obtain the DRAM memory cell having an amplifying function by a method wherein the SOI transistor on an insulating film and the source region of a switching transistor are connected to a bit wire, the drain region of the SOI transistor is connected to a source voltage, and the potential of a word wire and the bit wire are properly controlled.

CONSTITUTION: The switching transistor Q1 is an N-channel **MOSFET**, a polycrystalline silicon electrode 28, which is connected to a drain 24 of the transistor Q(sub 1), is formed on the **gate electrode** 25 of the transistor Q(sub 1) through the intermediary of a thin insulating film 27, and the **gate electrode** 25 is turned into a word wire. A P-channel **MOSFET** is the SOI transistor Q(sub 2) formed on the insulating film, the source 31 of the transistor Q(sub 2) is brought to come in contact with the source 23 of the transistor Q(sub 1), it forms a **P-N** junction **diode** , and it is also connected to a bit wire 34. As the switching transistor of the DRAM memory cell and the transistor for information read out are formed into an overlapped structure as above-mentioned, a memory cell having an amplifying function with the least occupation area can be obtained.

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32/3,AB/9 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

01692475
MANUFACTURE OF VERTICAL **MOSFET**

PUB. NO.: 60-170975 [JP 60170975 A]
PUBLISHED: September 04, 1985 (19850904)
INVENTOR(s): YAMAMOTO MASANORI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-027483 [JP 8427483]
FILED: February 16, 1984 (19840216)
JOURNAL: Section: E, Section No. 373, Vol. 10, No. 8, Pg. 47, January 14, 1986 (19860114)

ABSTRACT

PURPOSE: To provide the **MOSFET** with protective capacity while preventing the parasitic thyristor effect from happening by a method wherein an island region insulated and separated by an insulating film is formed making a semiconductor single crystal layer grow on the island region to form a protective diode.

CONSTITUTION: An oxide film 2 is formed on an N type Si substrate 1 to be provided with a window utilizing a photoresist 20 and then an insulating film 11 and an island region 22 encircled by the film 11 are formed by implanting oxygen ion 2 in the window. Firstly an Si single crystal film 23 and a polycrystalline Si layer 23' are respectively formed on the region 22 and the film 2 by means of depositing Si with the same conductive type as that of **region** (**N** type in this case). Secondly the layer 23 is left only on the region 22 while leaving a **gate electrode** of a vertical type **MOSFET** on the film 2. Finally a P type impurity is introduced to form **P** type **regions** 24a, 24c and **N** type **region** 24b. Through these procedures, a **P-N**-P Zener **diode** with protective capacity sufficient for a semiconductor layer with its thickness increased by the layer 23 so far deposited may be formed without fail.

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32/3,AB/10 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

01080385
SOLID-STATE IMAGE PICKUP DEVICE

PUB. NO.: 58-017785 [JP 58017785 A]
PUBLISHED: February 02, 1983 (19830202)
INVENTOR(s): KUBOTA KATSUHIKO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-115091 [JP 81115091]
FILED: July 24, 1981 (19810724)
JOURNAL: Section: E, Section No. 171, Vol. 07, No. 94, Pg. 88, April 20, 1983 (19830420)

ABSTRACT

PURPOSE: To enlarge the effective focussing area and improve the working property at the time of manufacturing and the integrating degree, by configuring the light receiving section with the light receiving surface at the opposite side of the electric circuit with burried type diodes.

CONSTITUTION: On a transparent substrate 1 of sapphire, GaP, etc., the 1st and 2nd P type epitaxial layers 2 and 3 are successively formed, and an N(sup +) type burred layer 4 is formed for a wide area between the two layers 2 and 3. A **P-N** junction **diode** 5 for light reception is configured by the junction of the layers 4 and 2. Moreover, an **MOSFET** 6 for switching is installed to the layer 3 and its source area 7 is deeply formed in the direction of thickness of the layer 3. A drain area 9 is formed to the layer 3 in such a way that the area 9 faces to the region 7 with a **gate electrode** 8 in between, and signals of each picture element are fetched by a signal taking-in line 10 made of Al and contacting on the area 9. A light 11 is irradiated into the picture element from the substrate 1, and carriers are gathered in the layer 4, and then, the output is outputted from the line 10 after it is selected by the FET6. Then, the effective focussing area is enlarged and, at the same time the manufacture is made easier.

32/3,AB/11 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

01041769
INSULATED GATE FIELD EFFECT SEMICONDUCTOR DEVICE

PUB. NO.: 57-192069 [JP 57192069 A]
PUBLISHED: November 26, 1982 (19821126)
INVENTOR(s): YAMAMOTO AKIRA
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-076580 [JP 8176580]
FILED: May 22, 1981 (19810522)
JOURNAL: Section: E, Section No. 159, Vol. 07, No. 40, Pg. 58, February 17, 1983 (19830217)

ABSTRACT

PURPOSE: To contrive to reduce the occupying area of element and to reduce the size of an insulated gate field effect semiconductor device by a method wherein the source or drain region of the second MISFET is connected directly to the source or drain region of the first MISFET with the reverse conductive region.

CONSTITUTION: The N(sup +) type semiconductor region 3, 4 and an N(sup +) type Si **gate electrode** 6 are provided in the region surrounded with SiO(sub 2) films 2 on the surface of a P type Si substrate 1, and an N channel **MOSFET** Q(sub 3) or Q(sub 4) is provided. A polycrystalline Si layer 7 for formation of the P channel **MOSFET** Q(sub 1) or Q(sub 2) is provided from the upper part of the film 2 being at the neighborhood of the **MOSFET** up to the position coming in contact directly with the drain region 3 of the FET Q(sub 3) or Q(sub 4). The P(sup +) type source region 8 and drain region 9 are provided in the layer 7 thereof. The reverse conductive type (**N**(sup +) type) **region** 12 is provided in the layer 7 in the condition coming in contact with the region 9, andf moreover connected directly to the **region** 3. A **P-N** junction **diode** D(sub 1) or D(sub 2) is formed by existence of the region 12 thereof between the region 9, and the regions 9, 3 are connected directly through the diode D(sub 1) or D(sub 2).

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32/3,AB/12 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

00987879
SEMICONDUCTOR DEVICE

PUB. NO.: 57-138179 [JP 57138179 A]
PUBLISHED: August 26, 1982 (19820826)
INVENTOR(s): FUTAMURA YASUO
WAKIMOTO HARUMI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-023021 [JP 8123021]
FILED: February 20, 1981 (19810220)
JOURNAL: Section: E, Section No. 144, Vol. 06, No. 238, Pg. 37, November 26, 1982 (19821126)

ABSTRACT

PURPOSE: To increase electrostatic destruction strength of a protection resistor, by inserting a junction diode as deep as a semiconductor region where the protection resistor is formed between a terminal and the protection resistor where the highest voltage in such semiconductor device as ROM is applied.

CONSTITUTION: A **P** type well **region** 2 is diffused and formed on an N type Si- substrare 1. A **P** type **region** 3 with the same depth is provided around it at the same time. An **N** type source **region** 4 and a drain region 5 of **MOS-FETs** , which constitute the first stage inverter, an **N**(sup +) type **region** 6 of input protection resistor, and an **N**(sup +) type **region** 7 facing to it are diffused and formed in the region 2. Next, a polycrystalline Si **gate electrode** 8 is connected to one end of the region 6. The other end is connected to an input terminal V(sub in) by an Al wiring 9. The wiring 9 is connected to the region 3 on the way to the terminal V(sub in). This creates a **P-N** junction **diode** between the terminal V(sub in) and a resistor 6, and clamps the high voltage V(sub ss) applied to the resistor 6.

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32/3,AB/13 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

00887569

# SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 57-037869 [JP 57037869 A]
PUBLISHED: March 02, 1982 (19820302)
INVENTOR(s): IWAMATSU SEIICHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-114168 [JP 80114168]
FILED: August 20, 1980 (19800820)
JOURNAL: Section: E, Section No. 113, Vol. 06, No. 107, Pg. 58, June 17, 1982 (19820617)

## ABSTRACT

PURPOSE: To obtain an inverter by connecting a **p-n** junction in series to a **MOSFET** or a bi-polar transistor.

CONSTITUTION: An n type source 11 and an n type drain 12 are made on a p type Si substrate 10 and a p layer 13 is formed in the source 11. A poly Si **gate electrode** 15 is made on a gate oxide film 14 and covered with an insulation film 17. Then, a window is etched to provide an Al wire 18 thereon. With such an arrangement, an inverter is completed with a **p-n** junction **diode** as a load resistance. A high resistance load of about 10(sub 15)ω can be formed easily thereby reducing the occupation area thereof substantially. Thus, a high-level integrated circuit can be obtained.

35/3,AB/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014311850
WPI Acc No: 2002-132552/200218
Related WPI Acc No: 1997-344410; 2001-302463; 2002-132550; 2002-132551;
2002-132553; 2002-132554
XRPX Acc No: N02-100009

MIS type semiconductor device such as **MOSFET**, IGBT, bipolar transistor, and semiconductor **diode** has **gate electrode** provided via **gate** insulation film on surface of well, which is present between source region and drift region

Patent Assignee: FUJI ELECTRIC CO LTD (FJIE )
Inventor: FUJIHIRA T
Number of Countries: 001 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| GB 2355586 | A | 20010425 | GB 971204 | A | 19970121 | 200218 | B |
| | | | GB 20011031 | A | 20010115 | | |
| GB 2355586 | B | 20010530 | GB 971204 | A | 19970121 | 200218 | |
| | | | GB 20011031 | A | 20010115 | | |

Priority Applications (No Type Date): JP 967935 A 19960122
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| GB 2355586 | A | | 71 | H01L-029/78 | Derived from application GB 971204 |
| GB 2355586 | B | | | H01L-029/78 | Derived from application GB 971204 |

Abstract (Basic): GB 2355586 A
Abstract (Basic):

NOVELTY - A second conductive type well is opposite to a drain region (29) and in contact with a drift region (1). A first conductive type source region is spaced apart from the first conductive type drift path region via the second conductive type well. A **gate electrode** (21) provided via a gate insulation film (13) on a surface of the well which is present between the source region and the drift region,

DETAILED DESCRIPTION - The **gate electrode** extends over a number of **p-n** junction between the drift path regions (1) and compartment regions (2).

USE - In a semiconductor device with a large current capacity and a high breakdown voltage, such as a **metal-oxide semiconductor** field-effect transistor (**MOSFET**), an IGBT, a bipolar **transistor**, and semiconductor **diode**.

ADVANTAGE - Relaxes the relationship between the ON resistance and the breakdown voltage to enable an increase in the current capacity by a reduction in the ON resistance under the high breakdown voltage.

DESCRIPTION OF DRAWING(S) - The drawing is a cross-sectional view of the n-channel **MOSFET** according to the present invention.

drift region (1)
compartment regions (2)
insulation film (13)
**gate electrode** (21)
drain region (29)
pp; 71 DwgNo 12e/12

35/3,AB/2     (Item 2 from file: 350)

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DIALOG(R)File 350:Derwent WPIX
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014311849
WPI Acc No: 2002-132551/200218
Related WPI Acc No: 1997-344410; 2001-302463; 2002-132550; 2002-132552;
  2002-132553; 2002-132554
XRPX Acc No: N02-100008
  MIS type semiconductor device such as MOSFET, IGBT, bipolar
  transistor, and semiconductor diode has gate electrode
  provided via gate insulation film on surface of well between source
  region and drift region
Patent Assignee: FUJI ELECTRIC CO LTD (FJIE  )
Inventor: FUJIHIRA T
Number of Countries: 001  Number of Patents: 002
Patent Family:
Patent No     Kind   Date     Applicat No     Kind   Date     Week
GB 2355585     A   20010425  GB 971204        A   19970121  200218  B
                             GB 20011030      A   20010115
GB 2355585     B   20010530  GB 971204        A   19970121  200218
                             GB 20011030      A   20010115

Priority Applications (No Type Date): JP 967935 A 19960122
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
GB 2355585    A     71 H01L-029/78   Derived from application GB 971204

GB 2355585    B        H01L-029/78   Derived from application GB 971204

Abstract (Basic): GB 2355585 A
Abstract (Basic):
        NOVELTY - A p-type semiconductor substrate (4) includes an n-type
    well located with a drain region (19) and in contact with a drift
    region (14). A p-type source region (18) is spaced
    apart from the second conductive type drift path region (14) via the
    n-type well. A gate electrode (10,11) is provided via a
    gate insulation film (12) on the surface of the well between the source
    region and the drift region. A drift current flows in lateral
    direction.
        USE - In a semiconductor device with a large current capacity and a
    high breakdown voltage, such as a metal-oxide
    semiconductor field-effect transistor (MOSFET), an IGBT, a
    bipolar transistor, and semiconductor diode.
        ADVANTAGE - Relaxes the relationship between the ON resistance and
    the breakdown voltage to enable an increase in the current capacity by
    a reduction in the ON resistance under the high breakdown voltage.
        DESCRIPTION OF DRAWING(S) - The drawing is a cross-sectional view
    showing a p-channel vertically structured MOSFET according to the
    present invention.
        p-type semiconductor substrate (4)
        gate electrode (10,11)
        gate insulation film (12)
        drift region (14)
        p-type source region (18)
        drain region (19)
        pp; 71 DwgNo 10/12


 35/3,AB/3     (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
```

009590283
WPI Acc No: 1993-283829/199336
XRPX Acc No: N97-458690

Power vertical field effect transistor - has several **MOSFETs** connected in parallel in substrate with all drains in common, each associated with one diode which has same breakdown voltage as transistor

Patent Assignee: NEC CORP (NIDE )
Inventor: TAKAHASHI M
Number of Countries: 002 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 5198816 | A | 19930806 | JP 92256671 | A | 19920925 | 199336 | B |
| US 5686750 | A | 19971111 | US 92952292 | A | 19920928 | 199751 | |
| | | | US 94341318 | A | 19941117 | | |
| | | | US 96639433 | A | 19960429 | | |

Priority Applications (No Type Date): JP 91248575 A 19910927
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 5198816 | A | | 9 | H01L-029/784 | |
| US 5686750 | A | | 10 | H01L-029/76 | Cont of application US 92952292<br>Cont of application US 94341318 |

Abstract (Basic): JP 5198816 A
US 5686750 A

The semiconductor device includes an n-type semiconductor substrate. Source and **gate electrode** pads (18,22) make external connections. They are located on a principal surface of the substrate, separate from each other. A drain electrode (19) covers a rear surface of the substrate. A cell zone is formed in the principal surface at a separate location from the source and **gate electrode** pads. An insulating film (17) is positioned on the principal surface of the substrate. Contact holes are formed through the insulating film. A number of vertical **MOSFET** cells are formed in the cell zone and are connected in parallel with one another. Each **MOSFET** cell includes a drain region which is formed of the semiconductor substrate, in common with all **MOSFET** cells. Each cell also includes a **p**-type base **region** (15) in the substrate. Each base region is separate from the other base **regions**. An **n**-type source **region** (16) is formed in each base region. A **gate electrode** is formed adjacent to a respective contact hole in the insulating film at least above each base region and between the corresponding source and drain regions.

A channel is created in a surface area of each base region and between the corresponding source and drain regions. Each channel is controlled by an associated **gate electrode**. The source region of each **MOSFET** cell is connected to a source electrode via a respective contact hole formed in the insulating film. The source electrode is connected to the source **electrode** pad. The **gate electrode** is connected to the **gate electrode** pad. Several **diode** cells (9) are formed in the substrate and arranged to form only one array of diode cells along at least one portion of an outer edge of the cell zone. Each diode cell has an **n**-type first **region** and a **p**-type second **region** formed in the substrate. Each second region is separate from the second regions of the other diode cells and the base regions of the **MOSFET** cells. The second region is connected with the regions of the other diode cells and the base regions of the

**MOSFET** cells only with the source electrode via an respective contact hole formed in the insulating film. The second region of each diode cell and the base regions of the **MOSFET** cells have the same impurity concentration and depth so that they have the same breakdown voltage. They are located at the same constant intervals so that the diode and **MOSFET** cells are located at equal intervals. The diode cells prevent a breakdown caused by a turn-on of a parasitic bipolar transistor of the **MOSFET** cells.

Dwg.2a/3

35/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009190635
WPI Acc No: 1992-318071/199239
XRAM Acc No: C92-141271
XRPX Acc No: N92-243460

Monolithic semiconductor device - has VDMOS transistor and **MOSFET** contg. a main electrode of lower doping concn. than main **electrodes** in **transistor**

Patent Assignee: HARRIS CORP (HARO ); JONES F P (JONE-I)
Inventor: JACKOSKI C E; JONES F P; MANSMANN J G; NEILSON J M S; WRATHALL R S; YEDINAK J A
Number of Countries: 005 Number of Patents: 005
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 505191 | A1 | 19920923 | EP 92302392 | A | 19920319 | 199239 | B |
| US 5164802 | A | 19921117 | US 91672243 | A | 19910320 | 199249 | |
| JP 4343476 | A | 19921130 | JP 9241884 | A | 19920131 | 199302 | |
| EP 505191 | B1 | 19960821 | EP 92302392 | A | 19920319 | 199638 | |
| DE 69212868 | E | 19960926 | DE 612868 | A | 19920319 | 199644 | |
| | | | EP 92302392 | A | 19920319 | | |

Priority Applications (No Type Date): US 91672243 A 19910320
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 505191 | A1 | E | 8 | H01L-029/784 | |
| US 5164802 | A | | 6 | H01L-029/784 | |
| JP 4343476 | A | | 6 | H01L-029/784 | |
| EP 505191 | B1 | E | 8 | H01L-029/772 | |
| Designated States (Regional): DE FR GB | | | | | |
| DE 69212868 | E | | | H01L-029/772 | Based on patent EP 505191 |

Abstract (Basic): EP 505191 A

Device comprises: a VDMOS transistor having first and second main electrodes and a control electrode; a lateral **MOSFET** having first and second main electrodes and a control electrode, one of the first and second electrodes of the **MOSFET** has a lower doping concn. than that of the main electrodes of the VDMOS transistor.

Pref. one electrode having a lower concn. is connected to the control electrode of the VDMOS transistor by way of a metallic connection, forming a Schottky barrier **diode** with the **electrode**; the other electrode of the **MOSFET** is connected to one of the first and second electrodes of the VDMOS transistor.

Also claimed is a monolithic semiconductor device comprising: a substrate of N+ type material, an upper region of the substrate having a lower impurity doping concn. that a lower portion; a first **P+** type **region** formed in the upper region of the substrate; a second

**N+** material **region** formed in the first **P+** **region** so as to leave an annular ring of P+ around the second **region**; a third **P+** material **region** formed in the upper region of the substrate; a fourth **N-** material **region** formed in the third **P+ region**; a fifth **N+** material **region** formed in the third region so as to leave an annular ring of P+ around the fourth region; a layer of gate oxide overlying at least a portion of each of annular rings; metallic conductor means contacting at least a portion of the fourth region; a **gate electrode** overlying at least a portion of the gate oxide, pref. contacted by the metallic conductor.

USE/ADVANTAGE - Power **MOSFET** vertically diffused **MOS** (VDMOS) transistor having an integral circuit. The low concn. **n** **region** improves dV/dt capability.

Dwg.3/3

Abstract (Equivalent): EP 505191 B

A monolithic semiconductor device comprising a VDMOS transistor (Q1) having first and second main electrodes (D,S) and a control electrode (G1) a lateral **MOSFET** (Q2) having first and second main electrodes and a control electrode (G2), wherein one of said first and second electrodes of said lateral **MOSFET** has a lower doping concentration than that of said first and second main electrodes of said VDMOS transistor, characterised in that said one electrode having a lower concentration is connected to said control electrode of said VDMOS transistor.

Dwg.1/3

Abstract (Equivalent): US 5164802 A

Monolithic semiconductor device having a first conductivity type substrate with the upper region doped to a lower level. A second conductivity type layer is appied followed by a second region of first conductivity type leaving an annular ring of second conductivity type material around the second region.

A third region of second type material is applied to the upper region of the substrate. A fourth region of first type material with a low doping layer is applied to the third region of second type material. Finally a fifth region is formed in the third region of second type material leaving an annular ring of second type material around the fourth region. A metallic contact to the fourth region forms a Schottky barrier **diode** while a **gate electrode** overlies at least part of the gate oxide.

ADVANTAGE - Turn on of the DMOS is enhanced since no minority carriers flow through the PN junction.

Dwg.3/3

35/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04393420
POWER INTEGRATED CIRCUIT

PUB. NO.: 06-037320 [JP 6037320 A]
PUBLISHED: February 10, 1994 (19940210)
INVENTOR(s): YOSHIDA KAZUHIKO
APPLICANT(s): FUJI ELECTRIC CO LTD [000523] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-187172 [JP 92187172]
FILED: July 15, 1992 (19920715)
JOURNAL: Section: E, Section No. 1548, Vol. 18, No. 255, Pg. 30, May

16, 1994 (19940516)

ABSTRACT

PURPOSE: To prevent formation of parasitic **MOSFET** by preventing a conductor having potential variation from existing on a high-resistance semiconductor layer between the same conductivity type regions of a switching element and a Zener diode.

CONSTITUTION: A drain electrode 92 of power **MOSFET** 11 is in contact with a cathode region 2 of a Zener **diode,** an **electrode** 10 is in contact with an anode region 52, and a contact of the Zener diode 16 between a drain and a gate is made by being in contact with a **gate electrode** 7 of the **MOSFET** 11. The wiring for that contact is formed of an Al layer bypassing the outside of a source electrode 91 of the **MOSFET** 11. Accordingly, the wiring 20 does not exist on the surface of a semi-conductor layer 1 between a **P**(sup +) **region** 3 or a P(sup +) well 51 of the **MOSFET** 11 and a P(sup +) well 52 of the Zener diode 16. An extension part of the **gate electrode** 7 does not exist either in this area. Accordingly, no channel is formed between the P(sup +) well 52 and the P(sup +) well 51 or the **P**(sup +) **region** 3 and formation of parasitic **MOSFET** can be prevented.

35/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03926667
CONDUCTIVITY MODULATION **MOSFET**

| | |
|---|---|
| PUB. NO.: | 04-291767 [JP 4291767 A] |
| PUBLISHED: | October 15, 1992 (19921015) |
| INVENTOR(s): | SAKURAI KENYA |
| APPLICANT(s): | FUJI ELECTRIC CO LTD [000523] (A Japanese Company or Corporation), JP (Japan) |
| APPL. NO.: | 03-055202 [JP 9155202] |
| FILED: | March 20, 1991 (19910320) |
| JOURNAL: | Section: E, Section No. 1328, Vol. 17, No. 104, Pg. 27, March 03, 1993 (19930303) |

ABSTRACT

PURPOSE: To provide a reliable device that includes a clamping bipolar transistor, having a narrow base than the open base of an IGBT, so as to bypass abnormal voltage applied between collector and base of the IGBT to turn it on.

CONSTITUTION: A **p**-type base **region** 4, a **p**(sup +)-base **region** 5, and a **p**(sup +)-**region** 6 are formed selectively in an n(sup -)-layer 3. The **p**(sup +)-**region** 6 is deeper than the **p**(sup +)-base **region** 5. A polycrystalline silicon layer is deposited on an insulating film 10 extending from a gate oxide film 9. The polycrystalline silicon layer includes a **p**(sup -)-**region** 11 and an **n**(sup +)-**region** 12 which form a **diode**. A metallic **gate electrode** 15 connected with a gate terminal G is in contact with a **gate electrode** 8 and the **n**(sup +)-**region** 12. An aluminum electrode 16 is in contact with the **p** (sup +)-**region** and **p**(sup -)-**region** . A pnp bipolar transistor for clamping is formed of a p(sup +)-collector 1, an n(sup +)-buffer layer 2, an n(sup -)-layer 3, and a p(sup +)-layer 6.

35/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03629870
ELECTROSTATIC INDUCTION THYRISTOR

| | |
|---|---|
| PUB. NO.: | 03-292770 [JP 3292770 A] |
| PUBLISHED: | December 24, 1991 (19911224) |
| INVENTOR(s): | NISHIZAWA JUNICHI<br>SUZUKI SOHE |
| APPLICANT(s): | SEMICONDUCTOR RES FOUND [351933] (A Japanese Company or Corporation), JP (Japan) |
| APPL. NO.: | 02-095251 [JP 9095251] |
| FILED: | April 10, 1990 (19900410) |
| JOURNAL: | Section: E, Section No. 1184, Vol. 16, No. 130, Pg. 79, April 02, 1992 (19920402) |

ABSTRACT

PURPOSE: To simplify a drive circuit and a control circuit and to reduce the drive circuit in number of component parts by a method wherein a **MOS diode** on a **gate** and an insulated **gate transistor** formed between a gate and a cathode or a gate and an anode are integrated on the same chip.
CONSTITUTION: A **gate electrode** 25 formed on a **p**(sup +) **region** 31 through the intermediary of a gate insulating film 26 not only constitutes a **MOS** diode but also serves as the **gate electrode** of an insulated **gate transistor** which makes p(sup +) **regions** 31 and 32 serve as its source and drain respectively. A normally-on type **MOSFET** is connected between the gate and the cathode of an Si thyristor. The relation between the impurity concentration of an **n-region** 22 and a distance between a pair of the **p**(sup +) **regions** 31 is so set as to enable a depletion layer to pinch off a channel when a voltage is not applied to the **gate electrode**.

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35/3,AB/8 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

01491067
HIGH-SPEED SWITCHING DEVICE

| | |
|---|---|
| PUB. NO.: | 59-202667 [JP 59202667 A] |
| PUBLISHED: | November 16, 1984 (19841116) |
| INVENTOR(s): | TANAKA TOMOYUKI |
| APPLICANT(s): | HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan) |
| APPL. NO.: | 58-076154 [JP 8376154] |
| FILED: | May 02, 1983 (19830502) |
| JOURNAL: | Section: E, Section No. 304, Vol. 09, No. 65, Pg. 50, March 26, 1985 (19850326) |

ABSTRACT

PURPOSE: To enable switching operation at high speed at low ON voltage and by a low control input by connecting a **diode** between a **gate electrode** in an **MOS. FET** and a base in a transistor in the direction that the direction of rectification is directed toward the

**gate electrode** from the base.

CONSTITUTION: A region 15 functions as a vertical type n channel **MOS. FET** in which a metallic layer 9 is used as a **gate electrode** , a metallic layer 8 as a source electrode and a metallic layer 7 as a drain electrode. An n type silicon layer 41 serves as a source and an n type silicon layer 2 and a silicon base body layer 1 as drain layers. On the other hand, a region 16 functions as a vertical type n(sup +)-**p-n** -n(sup +) bipolar transistor in which a metallic layer 6 is used as an emitter electrode, the metallic layer 7 as a collector electrode and the metallic layer 8 as a base electrode. An n type silicon layer 42 serves as an emitter, a p type silicon layer 3 as a base and the n type silicon layer 2 and the silicon base body layer 1 as collectors in the **region** 16. The **p** type silicon layer 3 and an n type silicon layer 43 form a diode in a region 17.

35/3,AB/9 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

01342546
IMAGE PICKUP DEVICE

PUB. NO.: 59-054146 [JP 59054146 A]
PUBLISHED: March 28, 1984 (19840328)
INVENTOR(s): MIYATA YUTAKA
HOTTA SADAKICHI
CHIKAMURA TAKAO
YANO KOSAKU
OOTA YOSHIO
FUJIWARA SHINJI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-164637 [JP 82164637]
FILED: September 20, 1982 (19820920)
JOURNAL: Section: E, Section No. 255, Vol. 08, No. 149, Pg. 25, July 12, 1984 (19840712)

ABSTRACT

PURPOSE: To obtain an image pickup device not deteriorating the resolution even if the operating voltage of a photoconductive film is reduced by forming the photoconductive film with a **p-i-n** structure and varying the thickness or specific resistance of a (p) layer or (n) layer with high specific resistance by location.

CONSTITUTION: An n(sup +) area is formed on a p type semiconductor substrate 10 to make a diode 11. An n(sup -) well 12 constituting a CCD transfer means constitutes **MOSFET** together with the **diode** 11, a **gate** oxide film 13, and a **gate electrode** 14. An electrode 15 on one side of a photoconductive film 16 is insulated from a signal scanning circuit except part of the diode 11 by low-melting point glass 17 such as phosphorus silicate glass. An insulation layer 18 made of SiO(sub 2) with a grain size from tens A to several hundreds A is formed in the area on the photoconductive film 16, and In(sub 2)O(sub 3)(Sn) is formed on the photoconductive film 16 and an insulation film 16 by spattering deposition to make a transparent electrode 19, then light rays 20 enter through the transparent electrode 19 side.

35/3,AB/10 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

00884069
PROTECTIVE **DIODE** FOR INSULATED **GATE** FIELD-EFFECT **TRANSISTOR**

PUB. NO.: 57-034369 [JP 57034369 A]
PUBLISHED: February 24, 1982 (19820224)
INVENTOR(s): TANIGAWA YOSHIKI
APPLICANT(s): PIONEER ELECTRONIC CORP [000501] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-109460 [JP 80109460]
FILED: August 09, 1980 (19800809)
JOURNAL: Section: E, Section No. 112, Vol. 06, No. 103, Pg. 58, June 12, 1982 (19820612)

ABSTRACT

PURPOSE: To enable to apply a layer current as well as to obtain a small input capacity protective element, in which the large current can be applied, by a method wherein a reverse conductive region to be connected to an input gate and a high density region, which was floating formed surrounding the reverse conductive region, are provided on a low density substrate and a punch-through is given between abovementioned two regions.

CONSTITUTION: For example, in the process wherein a dipole **MOSFET** is formed on a P(sup -) substrate, an annular **P region** 34 is formed simultaneously with channel regions 32 and 33, and an **N region** 38 is formed in a region 34 when source and drain regions 37, 39 and 40 are formed. The input **gate electrode** G(sub 1) covering the channel 32 is spread out as far as above the regions 34 and 38, and connected to **N region** 38 through a selective oxide layer. Through these procedures, the abnormal voltage of the G(sub 1) is punched through between the regions 34 and 38, and the breakdown of the FET can be prevented. Also, as the withstand voltage can be controlled within the range between regions 34 and 38 and a low density substrate is used, the input capacity of the protective diode can be made smaller than the ordinary junction diode.

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35/3,AB/11 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

00776567
INSULATED GATE TYPE FIELD EFFECT SEMICONDUCTOR DEVICE

PUB. NO.: 56-096867 [JP 56096867 A]
PUBLISHED: August 05, 1981 (19810805)
INVENTOR(s): KIKUCHI MASANORI
INOUE TAIICHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-106938 [JP 80106938]
FILED: August 04, 1980 (19800804)
JOURNAL: Section: E, Section No. 79, Vol. 05, No. 167, Pg. 157, October 24, 1981 (19811024)

ABSTRACT

PURPOSE: To protect the insulated gate type field effect semiconductor against a surge voltage by connecting an **MOS gate** controlled **diode** having low breakdown voltage to the source or drain of the **MOSFET**.

CONSTITUTION: An N-channel **MOSFETT**(sub 1) having a gate oxide film 6 formed on a P type Si substrate 1 is formed, a **gate** controlled **diode** D(sub 1) having an N type layer 4, a P type inversion preventive layer 5, a gate oxide film 6', a polysilicon **gate electrode** 9 and an aluminum electrode 13 are formed, and the source 3 of the FETT(sub 1) is connected through an aluminum wire 12 to the N type layer 4. In this case the withstand voltage of the diode D(sub 1) is set lower than the T(sub 1). Since the withstand voltage utilizes the surface breakdown mechanism of the **P-N** junction controlled by the **gate electrode** according to this configuration, no difference of time constant exists for the breakdown mechanism. Accordingly, high voltage can be shut off by the protecting device, and the semiconductor device can be prevented from being damaged.

40/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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04038508 INSPEC Abstract Number: B9201-2560R-021
Title: Dual-**MOSFET** structure for suppression of kink in SOI **MOSFETs** at room and liquid helium temperatures
Author(s): Gao, M.-H.; Colinge, J.-P.; Lauwers, L.; Wu, S.-H.; Claeys, C.
Author Affiliation: IMEC, Leuven, Belgium
Conference Title: 1990 IEEE SOS/SOI Technology Conference. (Cat. No.90CH2891-0) p.13-14
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA vi+178 pp.
ISBN: 0 87942 573 3
U.S. Copyright Clearance Center Code: CH2891-0/90/0000-0013$01.00
Conference Sponsor: IEEE
Conference Date: 2-4 Oct. 1990 Conference Location: Key West, FL, USA
Language: English
Abstract: The dual-**MOSFET** structure proposed consists of two SOI **nMOSFETs** , T/sub 1/ and T/sub 2/, in series, but measured as a single device (T/sub 1/ to the source and T/sub 2/ to the drain) with a common **gate electrode**. The **N**/sup +/ **region** in between T/sub 1/ and T/sub 2/ is kept floating. This structure can confine the kink effect to the upper transistor T/sub 2/ and thus successfully keeps the lower transistor T/sub 1/ from undergoing pinch-off, impact ionization, and the kink effect. If the channel length of T/sub 1/ is longer than that of T/sub 2/, then T/sub 1/ will dominate the overall output characteristics of the device. As a result, the kink effect is eliminated from the overall output characteristics. This structure can also confine the parasitic bipolar effect only to the upper transistor T/sub 2/. Since the base hole current of T/sub 2/ will recombine in the common **N**/sup +/ **region**, it cannot reach the base region of the lower transistor T/sub 1/. Results of measurements and simulation are given.
Subfile: B

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40/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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03505591 INSPEC Abstract Number: B89075986
Title: Novel test structure to study location of breakdown for trench capacitor
Author(s): Kishi, K.; Yoshida, T.; Watanabe, T.; Tanaka, T.; Shinozaki, S.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Conference Title: ICMTS 1989. Proceedings of the 1989 International Conference on Microelectronic Test Structures (Cat. No.89CH2693-0) p. 245-50
Publisher: IEEE, New York, NY, USA
Publication Date: 1989 Country of Publication: USA xii+265 pp.
ISBN: 0 87942 714 0
U.S. Copyright Clearance Center Code: CH2693-0/89/0000-245$01.00
Conference Sponsor: IEEE; IEE
Conference Date: 13-14 March 1989 Conference Location: Edinburgh, UK
Language: English
Abstract: A test structure for detecting the location of the breakdown of a trench capacitor electrically is introduced. It is very important to know the location of the breakdown in order to improve oxide integrity. However, the conventional failure analysis method for a plane capacitor cannot be

applied to a trench capacitor. A vertical n-channel **MOS** transistor is formed in the trench. An n-type substrate and surface **n-type region** are used as source and drain, respectively. The side surface of the trench in a p-well acts as a channel region. If the gate potential is lower than the threshold voltage of the n-channel **MOSFET**, they are electrically separated from each other. The location of oxide breakdown in the trench can be detected by checking the leakage current between **gate electrode** and drain, p-well and source. All capacitors show breakdown at either the bottom or the top of trench, not the side.

Subfile: B

44/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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7321347 INSPEC Abstract Number: B2002-08-2560R-071
Title: A novel reaction-diffusion system based on minority-carrier transport in solid-state CMOS devices
Author(s): Asai, T.; Nishimiya, Y.; Amemiya, Y.
Author Affiliation: Dept. of Electr. Eng., Hokkaido Univ., Sapporo, Japan
Conference Title: 2001 International Semiconductor Device Research Symposium. Symposium Proceedings (Cat. No.01EX497) p.141-4
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA xiv+669 pp.
ISBN: 0 7803 7432 0 Material Identity Number: XX-2002-00451
Conference Title: 2001 International Semiconductor Device Research Symposium. Symposium Proceedings
Conference Sponsor: IEEE; Electron Devices Soc.; Army Res. Office; NSF; Army Res. Lab.; NASA; Electr. & Comput. Eng. Dept.; Univ. Maryland
Conference Date: 5-7 Dec. 2001 Conference Location: Washington, DC, USA
Language: English

Abstract: We propose a novel silicon device for imitating autocatalytic and dissipative phenomena of reaction-diffusion (RD) systems, using the minority carriers in semiconductors as diffusion substances. Thus, the diffusion of chemical substances in the RD system is imitated by that of the minority carriers. The chemical reaction, which results in the change of the concentration of the substances, is imitated by a reaction device. Numerical simulations show that the proposed RD device can successfully produce propagating waves in the same way as natural RD systems. Our results indicate that the proposed RD device will be a useful tool for developing novel hardware based on the RD mechanism.

Subfile: B
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44/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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02880381 INSPEC Abstract Number: B87032600
Title: Lateral HVIC with 1200-V bipolar and field-effects devices
Author(s): Chang, M.F.; Pifer, G.; Yilmaz, H.; Wildi, E.J.; Hodgins, R.G. ; Owyang, K.; Adler, M.S.
Author Affiliation: General Electric Co., Research Triangle Park, NC, USA

Journal: IEEE Transactions on Electron Devices vol.ED-33, no.12 p. 1992-2001
Publication Date: Dec. 1986 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/86/1200-1992$01.00
Language: English

Abstract: The feasibility of a 1200-V **lateral** n-**p-n** bipolar junction transistor, **p-n diode** and **lateral** **DMOSFET** has been demonstrated for the first time. The on-resistance for the 1200-V **DMOSFET** is 4 times less than its 1200 V n-p-n BJT counterpart. The major contribution to high BJT on-resistance comes from the series JFET pinch resistance.

Subfile: B

44/3,AB/3 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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04210235 Genuine Article#: RN490 Number of References: 8
Title: GALVANOMAGNETIC EFFECTS IN LATERAL **P(+)-N DIODE** STRUCTURE (Abstract Available)
Author(s): NEDEV N; SMIRNOV N
Corporate Source: INST SOLID STATE PHYS,TZARIGRADSKO CHAUSSEE 72/BU-1784 SOFIA//BULGARIA/
Journal: JOURNAL OF INTELLIGENT MATERIAL SYSTEMS AND STRUCTURES, 1995, V6, N4 (JUL), P573-577
ISSN: 1045-389X
Language: ENGLISH Document Type: NOTE

Abstract: The magnetic field influence on the operation of a **p(+)-n diode** structure with two base contacts on the upper surface which are laterally and symmetrically positioned relative to the injecting p(+) region has been studied using the finite difference method. This analysis is important for the design of bipolar magnetic field sensors. Results for the changes of the potential distribution and of the electron and hole concentrations caused by a magnetic field applied perpendicular to the device cross section are presented. The influence of some geometric (device thickness, distance between electrodes) and physical (carrier mobility, surface recombination rates) parameters on the device operation is studied.

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44/3,AB/4 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
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01520143 AAD9638344
DIELECTRICALLY ISOLATED HIGH VOLTAGE POWER DEVICES
Author: HUANG, YIH-SHYAN
Degree: PH.D.
Year: 1996
Corporate Source/Institution: NORTH CAROLINA STATE UNIVERSITY (0155)
Source: VOLUME 57/07-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 4600. 159 PAGES

High voltage power devices in dielectrically isolated (DI) structure for power integrated circuits (PICs) applications have been proposed in this research by extending the REduced SURface electric Field (RESURF) principle of junction isolation (JI) technology. With the new DI RESURF technique, thin silicon layer DI wafers made by the direct-wafer-bonding (DWB) method have been utilized successfully to fabricate various lateral high voltage power devices. JI devices were simultaneously fabricated and their characteristics were compared to the new DI device structures.

Extensive two-dimensional computer simulations and analytic derivation were performed to obtain relationship of the breakdown voltage to major DI structure parameters such as silicon layer thickness, isolating oxide thickness, drift region doping concentration, and drift region length. Experimental results showed that breakdown voltages over 700 volts could be obtained in **lateral p-i-n diode** structure.

The high voltage lateral insulated gate bipolar transistor (LIGBT) has been investigated as a demonstration of the DI RESURF principle. Three different LIGBT collector structures were studied. These are the conventional collector with n-buffer layer, a shorted-collector, and a hybrid Schottky collector. Higher forward voltage drop in all three collector structures of DI devices were found compared to the JI case, but

the switching speed of the DI devices was observed to be faster by an order of magnitude. The cause of these differences is due to the additional current flow that occurs into the substrate in the JI devices. With shorter turn-on pulse width, the turn-off time was greatly reduced as verified by measurement. In comparison with JI devices, DI'S have superior trade-off performance.

The lateral emitter switched thyristor (LEST), a new lateral MOS-gated device, was analyzed, designed, and fabricated in DI and JI technologies with three anode constructions. Two basic LESTs, the conventional and dual channel structures, were studied. The breakdown voltage of DI LESTs attained could be predicted by DI RESURF principle. Analogous to LIGBTs, the forward voltage drop of DI LESTs was slightly higher than that of JI devices, and DI's were faster in switching speed. High voltage current saturation has been observed up to 200 V in dual channel LEST. However, forward characteristic of dual channel LEST were slightly poorer than the conventional LEST due to the space needed for second channel. In addition, LESTs only showed comparable dc and switching characteristics to LIGBTS. This is attributed to a larger cell area required for incorporating the floating cathode in LEST structure and a considerable part of current flow through the **MOSFET** channel in LEST.

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 48/3,AB/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011590871
WPI Acc No: 1998-008000/199801
Related WPI Acc No: 1990-022713; 1990-246627; 1992-226082; 1997-535143
XRAM Acc No: C98-002760
XRPX Acc No: N98-006355
  CMOS integrated circuit production - used in buried channel MOSFETs
  with short channel length
Patent Assignee: DALLAS SEMICONDUCTOR CORP (DALL-N)
Inventor: HARRINGTON T E
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No     Kind   Date    Applicat No    Kind   Date     Week
US 5688722     A   19971118  US 88210242     A   19880623  199801  B
                             US 89372077     A   19890627
                             US 90555556     A   19900718
                             US 91700354     A   19910507
                             US 91769144     A   19910927
                             US 92899409     A   19920616

Priority Applications (No Type Date): US 89372077 A 19890627; US 88210242 A
  19880623; US 90555556 A 19900718; US 91700354 A 19910507; US 91769144 A
  19910927; US 92899409 A 19920616
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 5688722    A     11 H01L-021/336  CIP of application US 88210242
                                     Div ex application US 89372077
                                     Cont of application US 90555556
                                     Cont of application US 91700354
                                     Cont of application US 91769144
                                     CIP of patent US 4906588
                                     Div ex patent US 4943537
                                     Cont of patent US 5122474

Abstract (Basic): US 5688722 A
        Fabricating a CMOS integrated circuit comprises: (a) providing a
    monocrystalline semiconductor substrate including p-type and n-type
    well regions separated by an isolation region; (b) implanting the
    n-type well with acceptor dopants sufficient to set the threshold
    voltage of the PMOS transistors to a predetermined value, implantation
    being performed with a predetermined stopping distance to give a
    predetermined buried channel depth; (c) forming gate dielectric over
    the wells, and a patterned thin film gate electrode on the
    substrate with first portions extending over portions of the p-type
    well to define NMOS channel regions, and second portions extending over
    the p-type well to define PMOS channel regions; (d) encapsulating all
    exposed surfaces of the gate electrode, and implanting
    donor dopants into both wells to form n-type lateral field isolation
    regions near the surface of the p-type well adjacent the PMOS channel
    region, the implant being performed with a stopping depth which will
    provide a maximum net concentration of n-type dopants at approximately
    the same depth as the buried channel; (e) implanting donor dopants into
    the p-type well only to form lightly doped drain extension regions near
    the surface of the well adjacent the NMOS channel region; and (f)
    forming spacer filaments on the side walls of the gate
    electrode, and p-type source/drain regions in portions of the
    n-type well not covered by the gate electrode and spacer
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filaments, each one of the PMOS channel regions being separated from respective adjacent ones by **lateral** field isolation **regions** , and **n**-type source/drain regions in portions of the p-type well not covered by the **gate electrode** and spacer filaments, each one of the NMOS channel regions being separated from respective adjacent ones by lightly doped extension regions.

USE - Used in CMOS processing.

ADVANTAGE - Small geometry is possible.

Dwg.5/8

48/3,AB/2     (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010535523
WPI Acc No: 1996-032477/199604
XRPX Acc No: N96-027414

MOS-controlled thyristor with current saturation characteristics - has N-type emitter region formed in P-type base, radially inwardly spaced along edges defining channel with metal strap connecting emitter region to P-type base, emitter base junction reverse-biases during turn-off

Patent Assignee: INT RECTIFIER CORP (INRC )
Inventor: AJIT J S
Number of Countries: 007  Number of Patents: 008
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| GB 2290659 | A | 19960103 | GB 9512777 | A | 19950622 | 199604 | B |
| DE 19521751 | A1 | 19960201 | DE 1021751 | A | 19950614 | 199610 | |
| FR 2723259 | A1 | 19960202 | FR 957418 | A | 19950621 | 199613 | |
| US 5498884 | A | 19960312 | US 94265397 | A | 19940624 | 199616 | |
| JP 8051197 | A | 19960220 | JP 95157752 | A | 19950623 | 199617 | |
| SG 33386 | A1 | 19961018 | SG 95722 | A | 19950623 | 199649 | |
| IT 1275762 | B | 19971017 | IT 95MI1305 | A | 19950616 | 199826 | |
| GB 2290659 | B | 19980624 | GB 9512777 | A | 19950622 | 199827 | |

Priority Applications (No Type Date): US 94265397 A 19940624
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| GB 2290659 | A | | 47 | H01L-029/745 | |
| DE 19521751 | A1 | | 22 | H01L-029/739 | |
| US 5498884 | A | | 20 | H01L-029/74 | |
| JP 8051197 | A | | 16 | H01L-029/74 | |
| FR 2723259 | A1 | | | H01L-029/745 | |
| SG 33386 | A1 | | | H01L-029/745 | |
| IT 1275762 | B | | | H01L-000/00 | |
| GB 2290659 | B | | | H01L-029/745 | |

Abstract (Basic): GB 2290659 A

The thyristor comprises an N-type layer (114) and a highly doped P-type region (116) disposed on the under side of a lightly doped N-type layer (118). An anode electrode (112) which is coupled to the anode terminal (A) covers the highly doped (116). Within the lightly doped N-type layer is a P-type base (120) which also forms the source of the P-channel **MOSFET**. An N++type emitter region (122) is disposed within P-base (120) and is electrically shorted by a floating metal strap (124) on the upper surface of the device (unconnected to any electrode of the device).

The P-type base is surrounded by P regions (126,128) but is separated by relatively small regions of lightly doped N-type layer (118) which extends to the surface of the wafer to form respective

channel regions (130,132). A cathode electrode (134) makes ohmic contact to the P regions. A first insulated gate (138) overlies the channel region (130) and a second insulated gate (140) over lies the channel region (132) and part of P-type base (120) between the N++ emitter region and channel region (132) at the upper surface of the wafer.

USE/ADVANTAGE - For high voltage and current applications. Not limited by parasitic thyristor structure within device. Has superior turn-off and wider safe-operating area.

Dwg.2/9

Abstract (Equivalent): US 5498884 A

A MOS-controlled thyristor, comprising:

a wafer of semiconductor material having first and second spaced, parallel planar surfaces, at least a portion of the thickness of the wafer which extends from said first semiconductor surface comprising a relatively lightly doped N-type layer for receiving junctions, at least a portion of the thickness of said wafer which extends from said second semiconductor surface comprising a relatively highly doped P-type layer;

a P-type base formed in said relatively lightly doped N-type epitaxially deposited layer and extending from said first semiconductor surface to a first depth beneath said first semiconductor surface;

an N-type emitter region formed in said P-type base and extending from said first semiconductor surface to a second depth beneath said semiconductor surface which is shallower than said first depth to create an N-type emitter/P-type base junction, said N-type emitter region being radially inwardly spaced along said first semiconductor surface along edges of said P-type base, such that said edges of said P-type base extend to said first semiconductor surface, thereby defining a first channel region along a first of said edges, a metal strap being disposed on said first semiconductor surface and connecting said emitter region to said P-type base along a second of said edges;

first and second P-type regions formed in said relatively lightly doped N-type layer and extending from said first surface of said wafer, said first and second **P-type regions** being **laterally** spaced from said second and first edges of said P-type base, respectively, to form second and third channel regions in said relatively lightly doped N-type epitaxial layer;

first gate insulation layer means on said first semiconductor surface disposed at least on said second channel region;

first **gate electrode** means on said first gate insulation layer means and overlying said second channel region;

second gate insulation layer means on said first semiconductor surface disposed at least on said first and third channel regions;

second **gate electrode** means on said second gate insulation layer means and overlying said first and third channel regions;

anode electrode means connected to said P-type layer disposed on said second semiconductor surface; and

cathode electrode means connected to said first and second P-type regions on said first semiconductor surface.

Dwg.2/9

48/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010154567
WPI Acc No: 1995-055819/199508

XRAM Acc No: C95-025366
XRPX Acc No: N95-044007

**P/N** channel **lateral** double diffused **MOSFET** mfr. - by connecting n-type source domain and drain domain which are separated by predetermined distance using **gate electrode** in N channel LD **MOSFET**

Patent Assignee: SHARP KK (SHAF )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 6334136 | A | 19941202 | JP 93118349 | A | 19930520 | 199508 | B |

Priority Applications (No Type Date): JP 93118349 A 19930520
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 6334136 | A | | 10 | H01L-027/092 | |

Abstract (Basic): JP 6334136 A

The P/N channel LD **MOSFET** manufacturing method involves deposition of high impurity diffuse N type layers (2,12) on a P type substrate (1) with a small space left between them. Each of the P type impurity diffusion layers (5,15) and the N type impurity diffusion layers (6,16) are formed in the two N type layers. These diffusion layers has the intermediate impurity density concentration. One of these two portions of the layers corresponds to N channel LD **MOSFET** structure and the other corresponds to the P channel LD **MOSFET**. The N channel structure holds a N+ type source domain (8s) and a P+ type layer (9) in the P type impurity diffusion layer and a N+ type drain domain (8d) in the N type impurity diffusion layer. A **gate electrode** (7) is installed over these layers thereby connecting the N+ type source domain and the drain domain which are separated by a predetermined distance. Similarly, another **gate electrode** (17) connects a P+ type domain (19d) and a P+ type source domain (19s) of the P channel LD **MOSFET**.

ADVANTAGE - Enables high speed operation. Simplifies structure of LD **MOSFET**. Controls variation in threshold value of LD **MOSFET**.

Dwg.1/10

48/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010091411
WPI Acc No: 1994-359124/199445
XRPX Acc No: N94-281364

MOS semiconductor device preventing erroneous operation caused by parasitic bipolar transistor - has structured insulation layer supporting **gate electrode** with source zone on top isolated by another insulation layer

Patent Assignee: SIEMENS AG (SIEI )
Inventor: STRACK H
Number of Countries: 003 Number of Patents: 004
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| DE 4315723 | A1 | 19941117 | DE 4315723 | A | 19930511 | 199445 | B |
| JP 7015008 | A | 19950117 | JP 94119552 | A | 19940509 | 199512 | |
| US 5396088 | A | 19950307 | US 94240138 | A | 19940510 | 199515 | |
| DE 4315723 | C2 | 19951005 | DE 4315723 | A | 19930511 | 199544 | |

Priority Applications (No Type Date): DE 4315723 A 19930511

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| DE 4315723 | A1 | | 4 | H01L-029/784 | |
| JP 7015008 | A | | 3 | H01L-029/78 | |
| US 5396088 | A | | 4 | H01L-029/78 | |
| DE 4315723 | C2 | | 4 | H01L-029/78 | |

Abstract (Basic): DE 4315723 A

The source areas (14) of an MOS semiconductor device are arranged upon the side of the gaze electrode (4). The upper surface of the source regions are contacted by source electrode (6). The base region (5) borders the side of the source region and gaze electrode and contacts drain region (1).

The new structure prevents the flow of minority charges from drain region to the source electrode via the source region. Instead these charges flow directly through the base region bordering the **gate electrode**, towards the source electrode.

The same principle of construction can be used for trench-MOS, U-MOS or V-MOS transistors.

ADVANTAGE - Prevents switching on of parasitic bipolar transistor and thus, avoids effect known as ''second breakdown''.

Dwg.1/2

Abstract (Equivalent): DE 4315723 C

The **MOSFET** has a lightly doped n-type drain region (1) with a surface (2) on the source side covered by a structured insulating layer (3) under the **gate electrode** (4). More insulation (13) separates the gate from a source region (14) against which a lightly-doped **p**-type base **region** (5) abuts **laterally**.

The base region overlaps the gate and abuts against the drainer region. The source electrode (6) contacts the source region on the side remote from the gate. A more heavily doped n-type region (9) (for an IGBT, a p-type region) covers the opposite side of the semiconductor body.

ADVANTAGE - Conduction through the parasitic bipolar structure is prevented reliably, with limitation of the IGBT current gain to less than unity in all circumstances.

Dwg.1/2

Abstract (Equivalent): US 5396088 A

The MOS component on a horizontally oriented semiconductor body, comprises at least one drain zone in the horizontally oriented semiconductor body, at least one base zone on the horizontally oriented semiconductor body and at least one source zone. At least one **gate electrode** is disposed over the drain zone and electrically insulated from the source zone and the drain zone, the source zone being vertically stacked on and over the **gate electrode**.

A portion of the base zone extends to laterally adjoin the source zone next to the **gate electrode** and is electrically insulated from the **gate electrode**. A source electrode is electrically contacted with the source zone on a surface facing away from the **gate electrode**. Each of the drain zone and the **gate electrode** have respective planar surfaces, with the planar surface of the base zone overlaps the planar surface of the **gate electrode**.

ADVANTAGE - Reliably prevents activation of parasitic bipolar structure.

Dwg.1/2

48/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008060633
WPI Acc No: 1989-325745/198945
XRPX Acc No: N89-248001
Switchable power semiconductor with insulated gate bipolar transistors - has unit cells associated with MOS controlled thyristors turned-off by field-effect-controlled short-circuit
Patent Assignee: ASEA BROWN BOVERI AG (ALLM ); ASEA BROWN BOVERI A (ALLM )
Inventor: BAUER F
Number of Countries: 012 Number of Patents: 005
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 340445 | A | 19891108 | EP 89105333 | A | 19890325 | 198945 | B |
| JP 2012969 | A | 19900117 | JP 8999898 | A | 19890419 | 199009 | |
| US 4967244 | A | 19901030 | US 89334967 | A | 19890407 | 199046 | |
| EP 340445 | B1 | 19930825 | EP 89105333 | A | 19890325 | 199334 | |
| DE 58905355 | G | 19930930 | DE 505355 | A | 19890325 | 199340 | |
| | | | EP 89105333 | A | 19890325 | | |

Priority Applications (No Type Date): CH 881520 A 19880422
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 340445 | A | G | 7 | | |
| Designated States (Regional): AT BE CH DE FR GB IT LI NL SE | | | | | |
| EP 340445 | B1 | G | 8 | H01L-029/74 | |
| Designated States (Regional): AT BE CH DE FR GB IT LI NL SE | | | | | |
| DE 58905355 | G | | | H01L-029/74 | Based on patent EP 340445 |

Abstract (Basic): EP 340445 A

The MOS contro-led thyristor (MCT) responsible for the turn-off process is associated with an insulated gate bipolar transistor (IGBT) whose p-type emitter layer (9) and n-type base layer (8) are of continuous form. The heavily-doped p-type region (13) is bounded **laterally** by **p**-doped channel **regions** (12) and inlaid n+ doped source regions (11), which with the n-type base layer (12) form an n-channel **MOSFET**.

The IGBT unit cell guarantees the turn-off of the thyristor. **Gate electrodes** (3) are held pref. at the same potential so that adjacent MCT and IGBT unit cells are controlled by the same gate.

ADVANTAGE - Can be optimised easily with regard to channel length, and affords more flexibility in respect of layout of component.

3/3

Abstract (Equivalent): EP 340445 B

Power semiconductor component with turn-off facility in which (a) next to each other and connected in parallel in a semiconductor substrate (14) between an anode (A) and a cathode (K); (b) each of said first unit cells is constructed as an MOS-controlled thyristor (MCT = MOS Controlled Thyristor) which can be turned off by means of a field-effect-controlled short circuit; (c) each of the first unit cells comprises, between the anode and the cathode a layer sequence composed of a p+ -doped p-type emitter layer, an n-doped n-type base layer, a p-doped p-type base layer (7) and an n+-doped **n**-type emitter **region** (6) with **laterally** adjacent **n**-doped channel **regions** (5) and embedded p+-doped source regions (4); (d) in each of the first unit cells, the source regions, the channel regions and

the p-type base layer emerge next to each other at the cathode-side surface of the semiconductor substrate and in each case form an n-channel **MOSFET** with an insulated **gate electrode** (3) situated above it; and (e) additional means are provided which ensure the field effect controlled turning-on of the component; characterised in that (f) the additional means comprise second unit cells which, independently of the first unit cells, are arranged between the latter and are connected in parallel with the latter; (g) each of the second unit cells has the structure of a bipolar transistor with insulated gate (IGBT = Insulated Gate Bipolar Transistor), in which (h) each of the second unit cells comprises, between the anode and the cathode, a layer sequence composed of a p+ -doped p-type emitter layer, an n-doped n-type base layer, and a p+ -doped p-type region (13), embedded in the n-type base layer, with **laterally** adjacent **p**-doped channel **regions** (12) and embedded n+-doped source regions (11); (i) in each of the second unit cells, the source regions, the channel regions (1) and the n-type base layer emerge next to each other at the cathode-side surface of the semiconductor substrate and in each case form an n-channel **MOSFET** with an insulated **gate electrode** situated above it; (k) the source regions and the p+-type region are connected directly to the cathode via a cathode contact; and (i) the p-type emitter layers and the n-type base layers of both unit cells are in each case part of a common p-type emitter layer (9) or n-type base layer (8) respectively extending laterally over the semiconductor substrate.

(Dwg.1/3

Abstract (Equivalent): US 4967244 A

The component consists of a number of unit cells arranged parallel to each other. Each cell is a MOS- controlled thyristor (MCT) which can be switched off by a field-effect-controlled short circuit. Bipolar-transistor-with-insulated-gate (IGBT) cells connected in parallel with the MCT unit cells ensure switching on.

Each MCT unit cell has a sequence of heavily doped emitter and medium doped base layers of different conducting types forming a first conductivity-type-channel **MOSFET** with an insulated **gate electrode** above it. The IGBT unit cells form a second conductivity type-channel **MOSFET** with an insulated **gate electrode** above it. The p-type emitter layers and the n-type base layers of both elementary cells are in each part of a commen p-type emitter layer or n-type base layer respectively extending laterally over the semi-conducted substrate.

ADVANTAGE - Improved switch-on capability and increased flexibility in designing component

48/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004327381
WPI Acc No: 1985-154259/198526
XRPX Acc No: N85-116471

Combined bipolar field effect transistor resurf device - exhibits lower requirement for base drive current for ON-state resistance and lower internal power dissipation

Patent Assignee: PHILIPS GLOEILAMPENFAB NV (PHIG )
Inventor: SINGER B M; STUPP E H; YAYARAMAN B
Number of Countries: 006 Number of Patents: 005
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|

|  |  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|---|
| EP 146181 | A | 19850626 | EP 84201803 | A | 19841205 | 198526 | B |
| JP 60153163 | A | 19850812 | JP 84266066 | A | 19841217 | 198538 |  |
| CA 1220875 | A | 19870421 |  |  |  | 198720 |  |
| EP 146181 | B | 19890315 |  |  |  | 198911 |  |
| DE 3477313 | G | 19890420 |  |  |  | 198917 |  |

Priority Applications (No Type Date): US 83562145 A 19831216; US 83562144 A 19831216

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 146181 | A | E | 17 |  |  |

Designated States (Regional): DE FR GB NL

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 146181 | B | E |  |  |  |

Designated States (Regional): DE FR GB NL

Abstract (Basic): EP 146181 A

A p-type semiconductor substrate (11) has a lightly-doped (3.10.14) epitaxial buried layer (16) on its major surface, which is about thrity microns thick and is p-conductivity type. An n-type epitaxial surface layer (18), of doping concentration and thickness chosen according to the reduced surface field technique, is disposed in the buried layer (16). A surface adjoining p-conductivity base region (20) has a base electrode (22) and forms part of a vertical pnp transistor. A surface-adjoining n+ conductivity combined source-emitter region (24) is formed with a source-emitter electrode (26).

An n+conductivity drain collector region (28) is adjacent to the surface layer (18) and spaced from the base connected to an electrode (30). A **lateral** n-**p**-n bipolar transistor is formed integrally with a lateral **MOSFET**. A **gate electrode** (36) is formed on an insulating layer (34) over a part of the channel region (32) which is in the base region.

ADVANTAGE - 'On' resistance of device, compared with previous combined bipolar-field effect transistor, is between one tenth and one third of previous value. In addition device is faster and provides enhanced lateral isolation.

1/5

Abstract (Equivalent): EP 146181 B

A p-type semiconductor substrate (11) has a lightly-doped (3.10.14) epitaxial buried layer (16) on its major surface, which is about thrity microns thick and is p-conductivity type. An n-type epitaxial surface layer (18), of doping concentration and thickness chosen according to the reduced surface field technique, is disposed in the buried layer (16). A surface adjoining p-conductivity base region (20) has a base electrode (22) and forms part of a vertical pnp transistor. A surface-adjoining n+ conductivity combined source-emitter region (24) is formed with a source-emitter electrode (26).

An n+conductivity drain collector region (28) is adjacent to the surface layer (18) and spaced from the base connected to an electrode (30). A **lateral** n-**p**-n bipolar transistor is formed integrally with a lateral **MOSFET**. A **gate electrode** (36) is formed on an insulating layer (34) over a part of the channel region (32) which is in the base region.

ADVANTAGE - 'On' resistance of device, compared with previous combined bipolar-field effect transistor, is between one tenth and one third of previous value. In addition device is faster and provides enhanced lateral isolation. (17pp Dwg.No.1/5

48/3,AB/7 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

01603371
VERTICAL FIELD EFFECT TRANSISTOR AND MANUFACTURE THEREOF

PUB. NO.: 60-081871 [JP 60081871 A]
PUBLISHED: May 09, 1985 (19850509)
INVENTOR(s): YAMAMOTO MASANORI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-189513 [JP 83189513]
FILED: October 11, 1983 (19831011)
JOURNAL: Section: E, Section Number 342, Volume 09, Number 225, Pg. 26, September 11, 1985 (19850911)

ABSTRACT

PURPOSE: To completely eliminate a defect due to a parasitic thyristor effect by completely insulating a protective diode region made of a lateral Zener diode from a vertical field effect transistor forming region.

CONSTITUTION: An n(sup +) type silicon substrate 1 form forming a drain region of an N-channel **DMOSFET,** an n type epitaxial layer 2, a gate p type region 3, an n(sup +) type source region 4, a gate insulating film 5, a polycrystalline silicn electrode 6, source and drain electrodes 7, 8 and a field insulating film 9 are provided. p type regions 11, 12, 13 for forming **lateral p-n** -p type Zener diode region and an n type region 14, source and **gate electrodes** 17, 18 are provided in the p type well 10. The Zener diode region is completely encircled by an insulating film 15 and a semiconductor insulating layer 16, electrically completely insulated and isolated from the drain region of the vertical FET, and a parasitic thyristor is not inserted between the gate and the drain of the vertical FET.

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48/3,AB/8 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

00923664
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 57-073964 [JP 57073964 A]
PUBLISHED: May 08, 1982 (19820508)
INVENTOR(s): ENOMOTO HIROSHI
NAKAMURA TSUNEO
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-149294 [JP 80149294]
FILED: October 27, 1980 (19801027)
JOURNAL: Section: E, Section Number 124, Volume 06, Number 151, Pg. 97, August 11, 1982 (19820811)

ABSTRACT

PURPOSE: To eliminate leakage between the emitter and collector of a lateral transistor, by a method wherein an MOS gate is provided between the emitter region and the substrate collector region, and a potential to prevent in inversion of the base region under the gate is applied when the lateral transistor is in an inoperative state.
CONSTITUTION: In order to improve driving capacity, a **lateral N-P-N** transistor T(sub 4) is provided in a CMOS gate circuit

comprising, e.g., a PMOSFETT(sub 6) and an NMOST(sub 8). Between a substrate collector region 31 of the T(sub 4) and an emitter region 33 disposed adjacently thereto through a base region 32, a gate insulating film 35 and a **gate electrode** 36 provided in order to connect an **MOSFETT** (sub 5) with the transistor T(sub 4) in parallel. By connecting the **gate electrode** 36 of the T(sub 5) to an output terminal O(sub 2), the potential of the gate 36 is at ground level when the T(sub 4) is in an inoperative state with input terminals I(sub 3), I(sub 4) at VD level, thereby to make it possible to prevent an N type inversion layer from being induced in the base region. Thus, it is possible to improve the driving capacity of the CMOS circuit and lower the power consumption simultaneously therewith.

52/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

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5258326 INSPEC Abstract Number: B9606-2560H-018
Title: Lateral tunneling devices on GaAs (111)A and (311)A patterned substrates grown by MBE using only silicon dopant
Author(s): Ohnishi, H.; Hirai, M.; Fujita, K.; Watanabe, T.
Author Affiliation: ATR Opt. & Radio Commun. Res. Labs., Kyoto, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) Conference Title: Japan J. Appl. Phys. 1, Regul. Pap. Short Notes (Japan) vol.35, no.2B p.1168-71
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: Feb. 1996 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199602)35:2BL.1168:LTDG;1-4
Material Identity Number: C579-96005
Conference Title: 1995 International Conference on Solid State Devices and Materials (SSDM `95)
Conference Date: 21-24 Aug. 1995 Conference Location: Osaka, Japan
Language: English
Abstract: A lateral interband tunneling **transistor** with **gate**-controlled negative differential resistance characteristics is demonstrated for the first time on a GaAs(111)A patterned substrate. Si-doped GaAs layers are grown on GaAs(111)A and GaAs(311)A patterned substrates by molecular beam epitaxy to fabricate **lateral p-n** junctions. Both samples show interband tunneling diode characteristics. Furthermore, a **gate electrode** is fabricated on the (111)A sample. The lateral tunneling transistor shows a modulated peak current density that ranges from 0.41 to 0.90 mA/cm/sup 2/ by varying the gate voltage from -5.0 to 5.0 V at 77 K.
Subfile: B

Copyright 1996, IEE

52/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

(c) 2005 Institution of Electrical Engineers. All rts. reserv.

02078573 INSPEC Abstract Number: B83038927
Title: Submicron-gate self-aligned GaAs FET by ion implantation
Author(s): Matsumoto, K.; Hashizume, N.; Atoda, N.; Tomizawa, K.; Kurosu, T.; Iida, M.
Author Affiliation: Electrotech. Laboratory, Ibaraki, Japan
Conference Title: Gallium Arsenide and Related Compounds, 1982. Tenth International Symposium on Gallium Arsenide and Related Compounds p. 317-24
Editor(s): Stillman, G.E.
Publisher: IOP, Bristol, UK
Publication Date: 1983 Country of Publication: UK xvi+650 pp.
ISBN: 0 85498 156 X
U.S. Copyright Clearance Center Code: 0305-2346/83/0065-0317$02.25
Conference Sponsor: Air Force Office Sci. Res
Conference Date: 19-22 Sept. 1982 Conference Location: Albuquerque, NM, USA
Language: English
Abstract: A self-aligned GaAs FET employing a tungsten metal as the **gate electrode** and at the same time as a mask for the ion implantation for the n/sup +/-regions is reported. The transconductance of 255 mS/mm was observed with a 0.8 mu m-gate FET. It was found that the

implanted Se ions in the **n/sup +/-regions** diffuse **laterally** into the active region during the annealing. Dependence of the FET characteristics on the gate length, annealing time, and crystal orientation is investigated.
Subfile: B

52/3,AB/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011511998
WPI Acc No: 1997-489913/199745
XRAM Acc No: C97-156238
XRPX Acc No: N97-408043
Insulated **gate** bipolar **transistor** - has insulating layer with **gate electrode**, arranged on base layer from source region layer to drift layer
Patent Assignee: ABB RES LTD (ALLM )
Inventor: BAKOWSKI M; GUSTAFSSON U; HARRIS C
Number of Countries: 019 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 9736329 | A1 | 19971002 | WO 97SE531 | A | 19970326 | 199745 | B |
| US 5763902 | A | 19980609 | US 96637105 | A | 19960424 | 199830 | N |
| EP 890191 | A1 | 19990113 | EP 97915821 | A | 19970326 | 199907 | |
| | | | WO 97SE531 | A | 19970326 | | |

Priority Applications (No Type Date): SE 961172 A 19960327; US 96637105 A 19960424
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 9736329 A1 E 25 H01L-029/739
Designated States (National): JP US
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
EP 890191 A1 E H01L-029/739 Based on patent WO 9736329
Designated States (Regional): DE FR GB IT SE
US 5763902 A H01L-029/74

Abstract (Basic): WO 9736329 A

An IGBT comprises a drain, a highly doped p-type substrate layer, optionally a highly doped n-type buffer layer, a low-doped n-type drift layer, a p-type base layer, a highly doped n-type source region layer and a source. A trench is etched into the base layer. An insulating layer with a **gate electrode** is arranged on the base layer at least from the source region layer to the drift layer, so that upon applying a voltage to the **gate electrode**, a conducting inversion channel is formed in the base layer at the interface to the insulating layer for electron transport from source to drain. The insulating layer has a contact portion vertically separated from the source region layer and has the source applied on it for collecting holes injected from the substrate layer to the drift layer at a vertical distance from the source region layer.

The production of the IGBT is also claimed and consists of epitaxially growing the device layers, mesa etching to form a groove in the drift layer, epitaxially growing a p-type base layer in the groove, implanting n-type dopants into the surface of the base layer to form a highly doped n-type source **region laterally** separated from the drift layer, and applying the insulating layer with **gate**

**electrode** onto the base layer.

USE - As switching devices in high power applications.

ADVANTAGE - The IGBT has a simple structure and has a large rate operating area due to a high latch-up tolerance.

Dwg.2/7

52/3,AB/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004131865
WPI Acc No: 1984-277405/198445
XRAM Acc No: C84-117583
XRPX Acc No: N84-207067

Semiconductor ROM device - includes poly-silicon conductive layer which contacts MOS transistor memory cell drains and lies near and on **gate electrode**

Patent Assignee: TOSHIBA KK (TOKE )
Inventor: ARIIZUMI S; IWASE T; MASUOKA F
Number of Countries: 006 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 124115 | A | 19841107 | EP 84104787 | A | 19840427 | 198445 | B |
| JP 59201461 | A | 19841115 | JP 8375026 | A | 19830428 | 198501 | |
| US 4737835 | A | 19880412 | US 86919556 | A | 19861016 | 198817 | |
| US 4855248 | A | 19890808 | US 88143068 | A | 19880112 | 198939 | |
| EP 124115 | B | 19901024 | | | | 199043 | |
| DE 3483437 | G | 19901129 | | | | 199049 | |

Priority Applications (No Type Date): JP 8375026 A 19830428
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 124115 A E 20
Designated States (Regional): DE FR GB IT
EP 124115 B
Designated States (Regional): DE FR GB IT

Abstract (Basic): EP 124115 A

Read only memory semiconductor device comprises: n+ regions (12,13) formed in p substrate (11) forming drain and source of a MOS **transistor; gate** insulation film (21); **gate electrode** (14); **gate** insulation (22,23); n+ conductive layer (16) formed on one of the n+ regions and extending onto the gate insulation film (22,23); and third conductive layer (18) formed on n+ conductive layer (16).

Device is made by: forming p field insulation region in substrate (11); forming gate insulation (21); forming **gate electrode** (14); doping n impurity to form n regions (12,13); depositing insulating film (22); forming contact hole (15), forming patterned n conductive layer (16); forming insulating film (24) with contact hole (17); and forming patterned conductive layer (18). Layer (16) is pref. a CVD polySi layer which is either pre-doped or implanted.

USE - In contact method data writing. Device has a small memory cell area and high integration density.

4/6

Abstract (Equivalent): EP 124115 B

1. A semiconductor read only memory device comprising:

a pair of regions (12,13) of a first conductivity type formed in a semiconductor substrate (11) of a second conductivity type opposite to said first conductivity type, the pair of regions individually forming drain and source regions of a MOS transistor; a first insulation film (21) for gate insulation formed on said substrate; a first conductive layer (14) for a **gate electrode** (140) formed on said gate insulation film; a second insulation film (22,23) formed on said **gate electrode**; a second conductive layer (16) containing an impurity of said first conductivity formed to contact one of said pair of regions, the second conductive layer extending onto said second insulation film (22,23) which is on said **gate electrode**; a third insulation film (24) having a contact hole leading to said second conductive layer (16); and a third conductive layer (18) formed to establish contact with said second conductive layer via said contact hole of said third insulation film (24), characterised in that: said contact hole of the third insulation film is above a portion of said one of said pair of regions and an adjacent portion of said **gate electrode**; and said third conductivity layer (18) extends to said second conductive layer via said contact hole of said third insulation film, so that the third conductive layer contacts said second conductive layer above said one of the pair of regions and said **gate electrode**.

(12pp

Abstract (Equivalent): US 4737835 A

Read only memory semiconductor device consists of matrix of memory cells (10), with n+ regions (12) formed in the region of a P-type semiconductor substrate (11), while a **laterally** extending **N + region** (13) forms a common source for the cells in a row. **Gate electrodes** (14) extend between source and drain (12, 13) of each cell in a row. Drain regions are in contact with a second conductive layer (16) extending as common gate over the word line (14) or a first interconnection layer through contact holes (15). Data lines (18) are formed for each column while contacting memory cells for data to be written through contact holes (17). Field oxidation film (20) separates elements and gate insulation (21) lies under the word line (14). Further oxidation films (22-24) are incorporated and a layer (25) under field oxidation film (20) prevents formation of a parasitic inversion layer.

ADVANTAGE - Memory cells occupy small area using contact method for data writing.

(9pp

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52/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

01598954
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-077454 [JP 60077454 A]
PUBLISHED: May 02, 1985 (19850502)
INVENTOR(s): SHINOHARA MAMORU
TSUBONE HITOSHI
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-184520 [JP 83184520]
FILED: October 04, 1983 (19831004)
JOURNAL: Section: E, Section Number 340, Volume 09, Number 216, Pg. 127, September 03, 1985 (19850903)

ABSTRACT

PURPOSE: To enable to control the gain of a lateral transistor by implanting the same ions on the bases of lateral transistor simultaneously when implanting P type impurity ions on the gate of an insulated **gate** type MOS **transistor** for controlling the threshold voltage of the transistor when providing a **P-N**-P type **lateral** transistor and the MOS transistor on the same semiconductor substrate.

CONSTITUTION: An N type layer 3 is epitaxially grown on a P type Si substrate 1, the layer 3 is separated via an separating region 2 into two islands, one of which is used as a **P-N**-P type **lateral** bipolar transistor forming region and the other of which is used as an insulated **gate** type MOS **transistor** forming region. Then, to control the threshold voltage of the MOS transistor, B(sup +) ions are implanted to the gate to form a layer 9. Then, the ions are simultaneously implanted also to the base of the bipolar transistor. Thereafter, diffused regions 4, 5 are formed in normal way, and a **gate electrode** 7 made of polycrystalline Si is mounted on the MOS transistor.

54/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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02145234 INSPEC Abstract Number: A83114475, B83060501
Title: Detection of electronic defects in strip-heater crystallized silicon thin films
Author(s): Johnson, N.M.; Moyer, M.D.; Fennell, L.E.; Maby, E.W.; Atwater, H.
Author Affiliation: Xerox Palo Alto Res. Centers, Palo Alto, CA, USA
Conference Title: Laser-Solid Interactions and Transient Thermal Processing of Materials p.491-7
Editor(s): Narayan, J.; Brown, W.L.; Lemons, R.A.
Publisher: Elsevier, New York, NY, USA
Publication Date: 1983 Country of Publication: USA xvii+769 pp.
ISBN: 0 444 00788 1
Conference Sponsor: US DOE
Conference Date: 1-4 Nov. 1982 Conference Location: Boston, MA, USA
Language: English

Abstract: Electronic defects in strip-heater crystallized silicon thin films have been investigated with capacitance-voltage (C-V), deep-level spectroscopic, and scanning-electron microscopic techniques. For electrical characterization the crystallized silicon films were used to fabricate inverted metal-oxide-silicon capacitors in which degenerately doped bulk silicon substrates provided the **gate electrode**. High-frequency C-V characteristics yield effective fixed-charge densities in the oxide of <or=2*10/sup 11/ cm/sup -2/. Trap-emission spectra, recorded with deep-level transient spectroscopy on both p-type and n-type capacitors, indicate a continuous distribution of deep levels throughout the silicon bandgap. The si-SiO/sub 2/ interface is considered to be the principal source of this deep-level continuum, since the films are essentially single crystal with a low density of subgrain boundaries; the effective interface-state density is <or=2.5*10/sup 10/ eV/sup -1/ cm/sup -2/. A discrete energy level, detectable above the background continuum, appears in the upper half of the silicon bandgap; it may identify a point defect in the bulk of the silicon film with a spatially uniform density of approximately 1*10/sup 13/ cm/sup -3/. On **lateral p-n** junction diodes, electron-beam-induced-current images reveal enhanced diffusion of arsenic along structural defects intersecting the junction.

Subfile: A B

54/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015900615
WPI Acc No: 2004-058454/200406
XRPX Acc No: N04-047217

Lateral insulated gate bipolar **PMOS** device for high-voltage power device, has source, drift and drain regions which form bipolar transistor that operates to provide additional current path, when device is in ON state

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG ); US PHILIPS CORP (PHIG )
Inventor: LETAVIC T; PETRUZZELLO J; DUFORT B
Number of Countries: 103 Number of Patents: 003
Patent Family:
Patent No Kind Date Applicat No Kind Date Week

US 6661059 B1 20031209 US 2002261254 A 20020930 200406 B
WO 200430105 A1 20040408 WO 2003IB4130 A 20030917 200425
AU 2003260893 A1 20040419 AU 2003260893 A 20030917 200462

Priority Applications (No Type Date): US 2002261254 A 20020930
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6661059 B1 5 H01L-029/76
WO 200430105 A1 E H01L-029/739
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW
AU 2003260893 A1 H01L-029/739 Based on patent WO 200430105

Abstract (Basic): US 6661059 B1
Abstract (Basic):

NOVELTY - A semiconductor-on-insulator (SOI) layer (26) includes a **p**-type source **region** (28), a **n**-type body **region** (30), a **n**-type **lateral** drift region (32) having a linearly graded charge profile increasing in doping level from drain to source, a **gate electrode** (36) and an insulation region (38). The source, drift and drain regions form a bipolar transistor that operates to provide an additional current path, when **PMOS** device is in the ON state.

USE - Lateral insulated gate bipolar **PMOS** device for high-voltage power devices.

ADVANTAGE - Provides additional current path and effectively reduces the on-resistance of the device, while the combination of the enhanced performance characteristics e.g. current flow and the on-resistance, makes the device suitable for operation in high voltage, high-current and in high breakdown voltage.

DESCRIPTION OF DRAWING(S) - The figure shows a cross- sectional view of the lateral insulation gate bipolar **PMOS** device.

SOI layer (26)
source region (28)
body region (30)
lateral drift region (32)
n-type drain region (34b)
**gate electrode** (36)
insulation region (38)
pp; 5 DwgNo 2/3

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54/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015087128
WPI Acc No: 2003-147646/200314
XRAM Acc No: C03-038058
XRPX Acc No: N03-116598
N-type **metal oxide semiconductor** transistor structure for integrated circuits, includes specified region underlying a p-well region
Patent Assignee: MITROS J C (MITR-I); TODD J R (TODD-I); WU X (WUXX-I)

Inventor: MITROS J C; TODD J R; WU X
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020149067 | A1 | 20021017 | US 2001833335 | A | 20010412 | 200314 | B |

Priority Applications (No Type Date): US 2001833335 A 20010412
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020149067 | A1 | | 19 | H01L-021/332 | |

Abstract (Basic): US 20020149067 A1
Abstract (Basic):

NOVELTY - An n-type **metal oxide semiconductor** ( **NMOS**) transistor structure comprises a PDUF (sic) region underlying a p-well region. The PDUF region exhibits a lesser resistivity than the p-well region and lowers a resistance associated with the p-well region at high drain voltages.

DETAILED DESCRIPTION - An **NMOS** transistor structure comprises:

(i) a p-well region in a semiconductor substrate;
(ii) an n-type source region (122) in the p-well region;
(iii) an n-type drain **region** in the **p**-well **region** and **laterally** spaced apart from the source region defining a p-type channel region;
(iv) a gate comprising a **gate electrode** (120) and a gate oxide overlying the channel region (136); and
(v) a PDUF region underlying the p-well region.

The PDUF region exhibits a resistivity which is less than the p-well region and lowers a resistance associated with the p-well region at high drain voltages, thus lowering a gain associated with a parasitic bipolar transistor, and increasing an injection induced breakdown voltage characteristic of the transistor structure.

An INDEPENDENT CLAIM is included for a method of forming the **NMOS** high voltage transistor structure.

USE - For integrated circuits.

ADVANTAGE - The device has an improved injection induced breakdown voltage characteristic.

DESCRIPTION OF DRAWING(S) - The figure shows a fragmentary cross section diagram of an **NMOS** transistor structure.

**Gate electrode** (120)
N-type source region (122)
Lightly doped drain high voltage region (127)
Channel region (136)
N-well region (146)
Contact region (148)
pp; 19 DwgNo 4/17

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54/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011728959
WPI Acc No: 1998-145869/199813
XRAM Acc No: C98-047763
XRPX Acc No: N98-115395

Fabrication of **MOS** transistors with selectively doped channel region - with lower threshold voltage and higher maximum drain current, I - Dsat

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI )
Inventor: FULFORD H J; GARDNER M I; HAUSE F N
Number of Countries: 003 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 9806137 | A1 | 19980212 | WO 97US13947 | A | 19970807 | 199813 | B |
| US 5804497 | A | 19980908 | US 96695101 | A | 19960807 | 199843 | |

Priority Applications (No Type Date): US 96695101 A 19960807
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 9806137 | A1 | E | 28 | H01L-029/78 | |
| Designated States (National): JP KR | | | | | |
| US 5804497 | A | | | H01L-021/70 | |

Abstract (Basic): WO 9806137 A

**MOS** transistor comprises: a) silicon substrate with a gate dielectric and then a **gate electrode** formed on it, b) first impurity distribution in the substrate formed parallel to its upper surface and with a peak concentration of first impurity at a first depth below the surface and acting as a channel stop and, c) a second impurity concentration parallel to the surface with a peak concentration at a second depth not as deep as the first and increasing the punch through voltage without substantially increasing the threshold voltage.

Also claimed (II) is a method of doping a channel region by: A) forming at least on n-channel **region laterally** displaced from at least one p-channel region, B) implanting first and second p-type impurities into the n-channel at first and second energy and dose, C) rapid thermal annealing the substrate to repair damage, and D) implanting first and second n-type impurities into the p-channel at first and second energy and dose, flowed by rapid thermal annealing.

USE - Fabrication of **MOS** transistors.

ADVANTAGE - Increasing ID sat increases the circuits performance by enabling each transistor to drive subsequent stages of transistors to their threshold voltage in less time.

Dwg.1/6

54/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007500789
WPI Acc No: 1988-134722/198820
XRPX Acc No: N88-102524

High-voltage high-performance monolithically integrated circuit - has power VDMOS transistor, **P-MOS** transistor, NPN transistor and PNP transistor on same chip together with low-leakage diodes

Patent Assignee: SGS MICROELETTRONICA SPA (SGSA )
Inventor: ANDREINI A; CONTIERO C; GALBIATI P
Number of Countries: 007 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 267882 | A | 19880518 | EP 87830379 | A | 19871027 | 198820 | B |
| JP 63296367 | A | 19881202 | JP 87284097 | A | 19871110 | 198903 | |
| IT 1201856 | B | 19890202 | | | | 199121 | |

Priority Applications (No Type Date): IT 8683657 A 19861110

Patent Details:

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Patent No  Kind Lan Pg   Main IPC    Filing Notes
EP 267882     A  E  22
   Designated States (Regional): DE FR GB NL SE
```

Abstract (Basic): EP 267882 A

An enhancement type polysilicon gate, junction-isolated N-channel VDMOS transistor has an N+ type source region, a P+type central body **region** and **P** type **lateral** body extension regions self-aligned with polysilicon **gate electrode** and polysilicon field plates extended over surrounding field oxide structure. N-type drain epitaxial layers connect by a N+ buried layer (3) and N+ xxxxxx diffusion (6t) (6b) with a drain electrode (D). An enhancement-type junction-isolated P-channel **MOS** transistor (H.V.P-CH **MOS**) is formed housing a P-type source extension region self-aligned with a relative **gate electrode**. P-type drain extension regions are formed on either side of a P+ central drain region. The extension regions are self-aligned with a polysilicon **gate electrode** and surrounding field oxide structure.

The reverse breakdown voltage of the **MOS** transistor is increased by the drain extension regions, to exceed the reverse breakdown voltage of the VDMOS transistor.

USE - Control of DC motor stepper motor operating at high currents and high switching frequency

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54/3,AB/6     (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03371476
MANUFACTURE OF VERTICAL TYPE FIELD EFFECT TRANSISTOR

| | |
|---|---|
| PUB. NO.: | 03-034376 [JP 3034376 A] |
| PUBLISHED: | February 14, 1991 (19910214) |
| INVENTOR(s): | SAWADA MASAMI |
| APPLICANT(s): | NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan) |
| APPL. NO.: | 01-169450 [JP 89169450] |
| FILED: | June 29, 1989 (19890629) |
| JOURNAL: | Section: E, Section Number 1060, Volume 15, Number 161, Pg. 110, April 23, 1991 (19910423) |

## ABSTRACT

PURPOSE: To control a gate cut-off voltage and to improve a transistor in latchup resistance by a method wherein at the formation of a base region, a high concentration base region is formed aligned with a **gate electrode**, the side face of the **gate electrode** is etched to make the **gate electrode** thin, and a low concentration base region is formed adjacent to the high concentration base region in an aligned manner.

CONSTITUTION: A polycrystalline silicon layer 4 is deposited on a gate oxide film 3, and an opening is provided. Then, a **gate electrode** 7 is built. Next, boron ions are implanted to form a high concentration p-type impurity injected region 8. Then, the side face of the **gate electrode** 7 at the opening 6 is etched to provided an undercut 9. Next, boron ions are implanted to form a low concentration impurity injected region 10. Then, a forced forming process is executed to provide a p(sup +)-type base region 11 to an n(sup -)-type epitaxial layer 2 of the opening 6 and a p(sup -)-type base region 12 adjacent to the base

region 11 respectively. Phosphorus ions are selectively implanted into the surface of the p(sup +)-type base region 11 and the p(sup -)-type base region 12 as partly aligned with the **gate electrode** 7 to form an **n**-type source **region** 13. The **lateral** etching of the **gate electrode** 7 is controlled in width so as to secure the base region 12 that the lateral diffusion of the p(sup +)-type diffusion region 11 produces no effect on a gate cutoff voltage.

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54/3,AB/7 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03285153
MANUFACTURE OF SEMICONDUCTOR INTEGRATED CIRCUIT

PUB. NO.: 02-260653 [JP 2260653 A]
PUBLISHED: October 23, 1990 (19901023)
INVENTOR(s): YAMAOKA TORU
APPLICANT(s): MATSUSHITA ELECTRON CORP [000584] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-083497 [JP 8983497]
FILED: March 31, 1989 (19890331)
JOURNAL: Section: E, Section Number 1020, Volume 15, Number 4, Pg. 65, January 08, 1991 (19910108)

ABSTRACT

PURPOSE: To form a highly reliable semiconductor integrated circuit by a method wherein a silicon oxide film and a silicon nitride film are continuously grown to form a composite film and an active base region is protected with the composite film from plasma damage.

CONSTITUTION: A composite film formed by growing continuously a silicon oxide film 22 and a silicon nitride film 23, which are formed by performing a selective etching or the like, is formed on an active base region of a **lateral** **P-N** -P transistor and moreover, a silicon oxide film 9 is selectively formed. Then, a continuously grown polycrystalline silicon film is selectively etched to form **gate electrodes** 10 and electrodes 24, with which the active base region is covered. After that, an emitter region, a collector region and the like are formed by an impurity implantation to form a bipolar transistor and the like. Thereby, the active base region is protected by the comsite film from damage due to plasma during production, a recombined current is inhibited and a reduction in a current amplification factor is prevented. Moreover, depletion and inversion of the vicinity of the surface of the active base region are prevented and a high-reliability semiconductor integrated circuit, in which there is no leakage current between the emitter and the collector, is formed.

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54/3,AB/8 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

02237722
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 62-154622 [JP 62154622 A]
PUBLISHED: July 09, 1987 (19870709)
INVENTOR(s): ISHIKAWA KATSUYA

APPLICANT(s): MATSUSHITA ELECTRONICS CORP [000584] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-293871 [JP 85293871]
FILED: December 26, 1985 (19851226)
JOURNAL: Section: E, Section Number 567, Volume 11, Number 390, Pg. 3, December 19, 1987 (19871219)

### ABSTRACT

PURPOSE: To improve the stability and the reliability of the characteristics of an element by ion implanting from many directions to distribute an impurity region in a laterally symmetrical manner.

CONSTITUTION: After a field oxide film (SiO(sub 2) film) 2 having approximately 0.6µm of thickness is selectively formed on a P-type silicon substrate 1 having a (100) plane and 10-15ωcm of specific resistance by an LOCOS method, a gate oxide film 3 having approximately 500 angstroms is formed, and a resist 5 on source.drain forming region is removed except the resist 5 on a **gate electrode** (poly-Si) 4 by photolithographic technique. When As ions are implanted with 140keV of acceleration energy in the quantity of 1X10(sup 16) pieces/cm(sup 2) from two directions, the distribution of source.drain **N**(sup +) type **regions** becomes **laterally** symmetrical. Here, the ion implanting directions are not limited to the two directions, and may be many directions that the distribution of the implanted region has a symmetry.

54/3,AB/9 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

01113372

## SEMICONDUCTOR DEVICE

PUB. NO.: 58-050772 [JP 58050772 A]
PUBLISHED: March 25, 1983 (19830325)
INVENTOR(s): MATSUBARA TOSHIAKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-147892 [JP 81147892]
FILED: September 21, 1981 (19810921)
JOURNAL: Section: E, Section Number 181, Volume 07, Number 136, Pg. 36, June 14, 1983 (19830614)

### ABSTRACT

PURPOSE: To obtain a lateral transistor available for the free trimming of the control of amplification factors and emitter dimensions, by controlling emitter currents by voltage impression onto a **gate electrode**.

CONSTITUTION: Since a P type inversed layer 5 is generated on the surface of an N(sup -) type Si substrate 1 under the gate by impressing a voltage onto the gate G and the area of a P(sup +) type emitter 3 increases resulting in the reduction of a substantial base width WB, and thereby the amplification factor hFE of the **lateral P-N**-P transistor fluctuates by the gate voltage VG. Further, a plurality of P(sup +) type emitters 3a, 3b are provided on the surface of an N(sup -) layer 9, the gate G is provided on the surface of the N(sup -) layer (base) between emitters via insulating films 4, the emitter area (peripheral length) is substantially increased by the P type inverted layer 5 generated by impressing a negative voltage onto the gate, and emitter currents are varied resulting in the fluctuation of the hFE. Thus, by providing an insulating **gate electrode** on the base and impressing a voltage thereon, the base width is varied resulting in the control of the hFE, and the N(sup -) layer is formed on the base surface resulting in the control of the hFE. Further, collector currents are varied by making the emitter area and the peripheral length variable, and thereby programmable elements or elements available for trimming can be obtained.

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 55/3,AB/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005  Thomson Derwent. All rts. reserv.

009787536
WPI Acc No: 1994-067389/199409
XRPX Acc No: N94-052757
  Adaptive-learning type product-sum operation circuit element - has single
  crystal semiconductor thin film with p-n-p or n-p-n structure
  in lateral direction formed in shape of stripes on insulator
  substrate and ferroelectric thin film for covering stripe
Patent Assignee: TOKYO INST TECHNOLOGY (TOKD  )
Inventor: ISHIHARA H
Number of Countries: 006  Number of Patents: 006
Patent Family:
Patent No     Kind   Date     Applicat No    Kind   Date     Week
EP 584844      A2  19940302  EP 93200856     A   19930325  199409  B
EP 584844      A3  19940824  EP 93200856     A   19930325  199531
US 5519812     A   19960521  US 9326779      A   19930305  199626
EP 584844      B1  19981223  EP 93200856     A   19930325  199904
DE 69322712    E   19990204  DE 622712       A   19930325  199911
                             EP 93200856     A   19930325
KR 139007      B1  19980615  KR 934555       A   19930324  200016

Priority Applications (No Type Date): JP 92224111 A 19920824
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
EP 584844     A2 E  16 G06F-015/80
   Designated States (Regional): DE FR GB NL
US 5519812    A      14 H01L-029/772
EP 584844     B1 E     G06F-015/80
   Designated States (Regional): DE FR GB NL
DE 69322712    E        G06F-015/80   Based on patent EP 584844
KR 139007     B1        G06G-007/60
EP 584844     A3        G06F-015/80

Abstract (Basic): EP 584844 A
        The product-sum operation circuit element has a single crystal
    semiconductor thin film (36,37) having a p-n-p or n-p-n structure in a
    lateral direction formed in the shape of stripes on the insulator
    substrate (35). A ferroelectric thin film is deposited on the substrate
    for covering at least the semiconductor stripe structure.
        A stripe-like gate electrode consists of a metal or a
    polycrystalline semiconductor for intersecting the semiconductor
    stripes at a right angle or suitable angle. A neuron circuit is
    included as a constituent element having an adaptive-learning function.
        ADVANTAGE - Circuit changes interval of output pulses by learning.
        Dwg.6/8
Abstract (Equivalent): US 5519812 A
        A product-sum operation circuit element comprising:
        an insulator substrate;
        at least one single crystal semiconductor thin film region on the
    insulator substrate, the at least one single crystal semiconductor thin
    film region extending in a first direction;
        a ferroelectric thin film deposited on the insulator substrate for
    covering at least the at least one single crystal semiconductor thin
    film region; and
        an electrode, formed on the ferroelectric thin film, the electrode
    extending in a second direction and crossing the at least one single
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crystal semiconductor thin film region;

wherein the at least one single crystal semiconductor thin film region includes first, second and third semiconductor thin film sections;

wherein the first and third sections are of a same conductivity-type and the second section is of a conductivity-type which is the opposite of the conductivity-type of the first and third sections; and

wherein the first, second and third semiconductor thin film sections are arranged along the second direction with the second section disposed between the first and third sections.

Dwg.7a/8

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55/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

01887964
**LATERAL** TYPE **P-N**-P-N ELEMENT

PUB. NO.: 61-102064 [JP 61102064 A]
PUBLISHED: May 20, 1986 (19860520)
INVENTOR(s): NEGORO TATSUO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-224606 [JP 84224606]
FILED: October 25, 1984 (19841025)
JOURNAL: Section: E, Section Number 440, Volume 10, Number 283, Pg. 95, September 26, 1986 (19860926)

## ABSTRACT

PURPOSE: To prevent the generation of leakage currents by forming structure in a shape that a conductor being in ohmic-contact with a cathode diffusion layer surrounds a gate diffusion layer through an insulating film.

CONSTITUTION: A boundary between an anode junction 1 and a semiconductor surface is coated with an anode electrode 8 through an insulating film 4. On the other hand, one part of a boundary between a gate junction 2 and the semiconductor surface is coated with a **gate electrode** 9 through the film 4. A cathode electrode 12 surrounds the whole boundary between the junction 2 and the semiconductor surface, and a channel between an anode and a gate is cut by the potential of the electrode 12. According to the structure, no channel is generated between the anode and a cathode, between the anode and the gate and between anode isolation junctions, thus reducing leakage currents.

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55/3,AB/3 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

01497177
SEMICONDUCTOR DEVICE

PUB. NO.: 59-208777 [JP 59208777 A]
PUBLISHED: November 27, 1984 (19841127)
INVENTOR(s): YOSHIHARA TOSHIO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 58-083067 [JP 8383067]
FILED: May 12, 1983 (19830512)
JOURNAL: Section: E, Section Number 305, Volume 09, Number 69, Pg. 151, March 29, 1985 (19850329)

## ABSTRACT

PURPOSE: To contrive improvement in the DC current amplification factor and the cut-off frequency of the titled semiconductor device by a method wherein said device is constituted in such a manner that a series circuit is formed by the emitter and the collector of a **horizontal** type **P-N** -P transistor and the source and the drain of a P-channel junction type FET.

CONSTITUTION: A P type first region 1 is provided on an N type semiconductor substrate 10, the second region 2 is provided outside the region 1, and a P type third region 3 is provided outside the region 2. Then, a P type fourth region 4 having the impurity density lower than that of the regions 2 and 3 is formed in the N type region located between the regions 2 and 3 adjoining to said regions. Then, an oxide film 5 is provided on the surface of a substrate 1, and electrodes 6-8 are formed. According to this constitution, a high withstand voltage can be obtained because a series circuit is formed by the emitter and the collector of a **horizontal** type **P-N** -P transistor TRT(sub 1) and the source and drain of a P-channel junction type FETT(sub 2). Also, the base electrode of the TRT(sub 1) and the **gate electrode** of the FETT(sub 2) are connected common, but the effect thereof can be neglected.

STIC Search

```
File 342:Derwent Patents Citation Indx 1978-05/200516
       (c) 2005 Thomson Derwent

 S1       4   PN=(US 0070388 OR US 6304484 OR US 5753952 OR US 5920091
                   OR US 5610409)
? MAP PN

SYSTEM:OS  - DIALOG OneSearch
  File 350:Derwent WPIX 1963-2005/UD,UM &UP=200519
         (c) 2005  Thomson Derwent
*File 350: For more current information, include File 331 in your search.
Enter HELP NEWS 331 for details.
  File 347:JAPIO Nov 1976-2004/Nov(Updated 050309)
         (c) 2005 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.

Set     Items   Description
S1         36   S1:S5
S2         10   S1 AND (MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS?
             ? OR N()MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ?
              OR C()MOS? ? OR CMOS? ? OR NMOSFET? ? OR NMOS()FET? ? OR PMO-
             S()FET? ? OR PMOSFET? ?)
S3         26   S1 NOT S2
S4          1   S3 AND (DMOS()FET? ? OR DMOSFET? ? OR UMOS()FET? ? OR UMOS-
             FET? ? OR MOS()FET? ? OR MOSFET? ?)
S5         25   S3 NOT S4

S7         23   S5 NOT S6
S8          2   S7 AND GATE(2N)ELECTROD?
S9         21   S7 NOT S8

S11         1   S9 AND DIODE(2N)(GATE()ELECTROD? OR GATE OR ELECTROD?)
S12        20   S9 NOT S11
S13        20   IDPAT (sorted in duplicate/non-duplicate order)
S14        15   IDPAT (primary/non-duplicate records only)
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 2/3,AB/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005  Thomson Derwent. All rts. reserv.

015219750
WPI Acc No: 2003-280662/200328
XRPX Acc No: N03-222797
  Integrated circuit memory cell avalanche injection MOS having
  single floating grid active surface saddling and memory point different
  voltages three logic programming levels providing.
Patent Assignee: STMICROELECTRONICS SA (SGSA  )
Inventor: CASPAR D; DRAY C; FOURNEL R
Number of Countries: 032  Number of Patents: 005
Patent Family:
Patent No      Kind   Date     Applicat No    Kind   Date      Week
EP 1289024      A1  20030305  EP 2002292109    A   20020828  200328   B
FR 2829279      A1  20030307  FR 200111381     A   20010903  200328
US 20030063498  A1  20030403  US 2002228164    A   20020826  200330
JP 2003152119   A   20030523  JP 2002252983    A   20020830  200343
US 6728135      B2  20040427  US 2002228164    A   20020826  200429

Priority Applications (No Type Date): FR 200111381 A 20010903
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
EP 1289024    A1 F   9 H01L-029/788
   Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
   GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR
FR 2829279    A1       G11C-016/04
US 20030063498 A1       G11C-007/00
JP 2003152119 A      6 H01L-021/8247
US 6728135    B2       G11C-016/00

Abstract (Basic): EP 1289024 A1
Abstract (Basic):
        NOVELTY - The integrated circuit memory cell has a single floating
    grid (GR) saddling (PF1,PF2) an active surface of a two profile
    semiconductor substrate, limiting the electrodes to the active zone.
    There is a memory point (SW) selectively applying different voltages to
    the electrodes providing three programming logic levels.
        USE - Floating gate avalanche injection FAMOS integrated circuit
    memory cell.
        ADVANTAGE - The memory cell has three levels of programming.
        DESCRIPTION OF DRAWING(S) - The figure shows the memory mechanism
        floating grid (GS)
        saddling (PF1,PF2)
        memory point (SW)
        pp; 9 DwgNo 1/2


 2/3,AB/2     (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013661523
WPI Acc No: 2001-145735/200115
XRPX Acc No: N01-106522
  Split gate oxide asymmetric MOS device for active circuits used in
  microprocessor, has gate electrode formed on notch of channel located
  inbetween source and drain on substrate
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Patent Assignee: SUN MICROSYSTEMS INC (SUNM  )
Inventor: BURR J B
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No     Kind   Date    Applicat No    Kind   Date     Week
US 6121666     A   20000919  US 97884152     A   19970627  200115  B

Priority Applications (No Type Date): US 97884152 A 19970627
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 6121666    A     18 H01L-029/76

Abstract (Basic): US 6121666 A
Abstract (Basic):
        NOVELTY - The channel (44) is located in the substrate between the
    source and drain of asymmetric MOS device. A dielectric layer
    (40) formed on channel, has gate electrodes in the notch (50) of
    channel region with lateral sections extending parallel to active
    surface on the substrate (52). The channel region underlying the
    lateral section of electrodes, has low and high threshold voltages.
        USE - Split gate oxide asymmetric MOS device for active
    circuits used in microprocessor.
        ADVANTAGE - Since the channel region of lower length is located
    between source and drain regions on the substrate, charge carriers are
    prevented from jumping across the channel.
        DESCRIPTION OF DRAWING(S) - The figure shows the side sectional
    view of split gate oxide asymmetric MOS device.
        Dielectric layer (40)
        Channel (44)
        Notch (50)
        Substrate (52)
        pp; 18 DwgNo 1A/4


 2/3,AB/3     (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005  Thomson Derwent. All rts. reserv.

011227717
WPI Acc No: 1997-205620/199719
XRPX Acc No: N97-169692
  Semiconductor memory with floating gate cells esp. DRAM - includes single
  stacked transistor as cell storage element, which is charged and
  discharged by MOS transistor formed with gate electrode over
  floating gates and between memory transistors control gates
Patent Assignee: LG SEMICON CO LTD (GLDS  ); GOLDSTAR ELECTRON CO LTD (GLDS
  ); HYUNDAI MICROELECTRONICS CO LTD (HYUN-N)
Inventor: PARK K H; PARK K; PARK G H
Number of Countries: 008  Number of Patents: 011
Patent Family:
Patent No     Kind   Date    Applicat No    Kind   Date     Week
EP 767498      A1  19970409  EP 96113764     A   19960828  199719  B
TW 300338      A   19970311  TW 96102839     A   19960308  199724
JP 9129837     A   19970516  JP 96281285     A   19961003  199730
US 5687119     A   19971111  US 96646152     A   19960507  199751
KR 97024197    A   19970530  KR 9534120      A   19951005  199824
US 5950088     A   19990907  US 96646152     A   19960507  199943
                             US 97879135     A   19970619
US 5998827     A   19991207  US 96646152     A   19960507  200004
                             US 97879317     A   19970619
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KR 179175      B1   19990320  KR 9534120      A   19951005  200043
CN 1147674     A    19970416  CN 96108646     A   19960626  200108
EP 767498      B1   20040114  EP 96113764     A   19960828  200406
DE 69631315    E    20040219  DE 631315       A   19960828  200419
                              EP 96113764     A   19960828
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Priority Applications (No Type Date): KR 9534120 A 19951005
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
EP 767498     A1 E  23 H01L-027/115
   Designated States (Regional): DE FR GB
TW 300338     A        H01L-027/108
JP 9129837    A     13 H01L-027/10
US 5687119    A     19 G11C-016/06
KR 97024197   A        H01L-027/108
US 5950088    A        H01L-021/8247 Div ex application US 96646152
                                     Div ex patent US 5687119
US 5998827    A        H01L-029/72   Div ex application US 96646152
                                     Div ex patent US 5687119
KR 179175     B1       H01L-027/115
CN 1147674    A        G11C-011/34
EP 767498     B1 E     H01L-027/115
   Designated States (Regional): DE FR GB
DE 69631315   E        H01L-027/115  Based on patent EP 767498
```

Abstract (Basic): EP 767498 A

The semiconductor memory includes memory cells with a floating gate storing an electric charge, with a **MOS** switching transistor charging the floating gate and switching to discharge the stored charge. The memory cells each include a control electrode for the charge storing and discharging operation. Pref. a memory cell includes two bit lines, with a sensing amplifier connected to each bit line. The memory cells are pref. arranged in a matrix, with the switching transistors of the same row connected in series and having floating drain terminals.

The memory cell floating gates (13) and control electrodes (14), which are located over each floating gate, are pref. formed mutually perpendicular to each other, with the transfer transistors (15) formed spaced at a constant pitch on each floating gate and between the respective control electrodes. The floating gates beneath the control electrode and the transfer transistor are pref. of opposite conductivity type. The transfer transistor programs and erases the memory cells.

ADVANTAGE - Reduced cell area, without capacitor; simplified mfg. process.

Dwg.6/14

Abstract (Equivalent): US 5687119 A

A semiconductor memory device comprising:

a plurality of memory cells each having a floating gate electrode; and

a plurality of switching elements for charging the floating gate electrode of each memory cell with an electric charge and for performing a switching function to discharge the electric charge;

wherein the plurality of switching elements are connected in series.

Dwg.5/14j

2/3,AB/4     (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007111442
WPI Acc No: 1987-111439/**198716**
Solid state image pick-up device - has two laminated photo sensing **MOS** transistor layers NoAbstract Dwg 1/4
Patent Assignee: MITSUBISHI DENKI KK (MITQ )
Number of Countries: 001 Number of Patents: 001
Patent Family:

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Patent No     Kind   Date     Applicat No    Kind   Date      Week
JP 62055961    A   19870311  JP 85198216     A   19850905  198716  B
```

Priority Applications (No Type Date): JP 85198216 A 19850905
Patent Details:

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Patent No   Kind Lan Pg   Main IPC    Filing Notes
JP 62055961   A      4
```

2/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05608953
NONVOLATILE MEMORY HAVING MULTIBIT CORRESPONDING CELL OF TWO-LAYERED FLOATING GATE STRUCTURE AND ITS PROGRAMMING/ERASING/READING METHOD

PUB. NO.: 09-223753 [**JP 9223753** A]
PUBLISHED: August 26, 1997 (19970826)
INVENTOR(s): KOJIMA TOSHIAKI
APPLICANT(s): NIPPON MOTOROLA LTD [489085] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-030779 [JP 9630779]
FILED: February 19, 1996 (19960219)

ABSTRACT

PROBLEM TO BE SOLVED: To increase storage capacity, by making a first floating gate and a control gate which are formed on a source and a drain a readout part, and making a second floating gate and a program gate which are formed on a high impurity concentration layer an erasing part.

SOLUTION: At the time of readout mode, the amount of a current flowing between a drain 3 and a source 2 is detected by applying a voltage to a control gate 5. The threshold voltage of a first floating gate 4A is detected by charges charged on second floating gates 4B(sub 1), 4B(sub 2), and stored information is read out. At the time of program mode, a voltage is applied to a program gate 6(sub 2), and the high impurity concentration layer 22 is grounded. Then FN tunneling is generated between a tunnel oxide film formation part 4B(sub 20) and the high impurity concentration layer 22, and implantation is performed to the second floating gate 4B(sub 2). At this time, implantation is not performed to the second floating gate 4B(sub 1) by an insulating layer 10.

2/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04417603
NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND ITS MANUFACTURE

PUB. NO.: 06-061503 [**JP 6061503** A]
PUBLISHED: March 04, 1994 (19940304)
INVENTOR(s): WAKE SETSUO
TAMURA KATSUHIKO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-215151 [JP 92215151]
FILED: August 12, 1992 (19920812)
JOURNAL: Section: E, Section No. 1558, Vol. 18, No. 299, Pg. 90, June 08, 1994 (19940608)

ABSTRACT

PURPOSE: To stabilize the writing and erasing operations to the storage device and improve the reliability of the device by positionally deviating the part where delivery and reception of electrons are performed at the writing and erasing time from a gate bird's beak.

CONSTITUTION: Source and drain diffusion areas 6 and 7 are formed on the main surface of a p-type semiconductor substrate 1 so as to specify a channel area. An impurity introducing layer 21 having its end section at a position farther from the channel area than the end sections of the areas 6 and 7 near the surface of the substrate 1 is formed on the substrate 1. Then a floating gate electrode 3 is formed on the substrate 1 with a gate insulating film 2 in between so that its end sections can step on the layer 21. In addition, a control gate electrode 5 is formed on the electrode 3 with an interlayer insulating film 4 in between.

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2/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

04022103
PHOTOELECTRIC TRANSFER DEVICE

PUB. NO.: 05-013803 [**JP 5013803** A]
PUBLISHED: January 22, 1993 (19930122)
INVENTOR(s): YAMADA KATSUHIKO
GOFUKU IHACHIROU
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-184164 [JP 91184164]
FILED: June 28, 1991 (19910628)
JOURNAL: Section: E, Section No. 1372, Vol. 17, No. 276, Pg. 135, May 27, 1993 (19930527)

ABSTRACT

PURPOSE: To obtain photoelectric transfer characteristics optimum for high density picture image reading further avoiding deterioration of the characteristics due to element isolation.

CONSTITUTION: Within the title photoelectric transfer device, a photoelectric transfer element part 13 and an amplifier element part 11 amplifying signals from the element part 13 are provided on a substrate 1; the photoelectric transfer element part 13 contains a photodiode as a photoelectric transfer layer; the amplifier element part 11 is composed of a MIS type transistor while the element part 13 is arranged on the element part 11; furthermore, the gate electrode layer 103 of the MIS type transistor in the amplifier element part 11 is commonly used as the lower electrode layer 103 of the photodiode in the photoelectric transfer element

part 13. At this time, a doped layer 106 extends farther than an upper electrode layer 107 seen from the normal direction to the substrate 1 surface in the photoelectric transfer element part 13. On the other hand, 110 and 111 respectively represent a source electrode layer and a drain electrode layer.

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2/3,AB/8 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

02139061
SOLID STATE IMAGE PICK-UP DEVICE

PUB. NO.: 62-055961 [**JP 62055961** A]
PUBLISHED: March 11, 1987 (19870311)
INVENTOR(s): HIROSE SATOSHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-198216 [JP 85198216]
FILED: September 05, 1985 (19850905)
JOURNAL: Section: E, Section No. 530, Vol. 11, No. 244, Pg. 106, August 08, 1987 (19870808)

ABSTRACT

PURPOSE: To prevent false signals from generating due to incident light among picture elements by forming picture elements for which is formed a photoelectric conversion means on an upper layer of a layer of picture elements for which a conversion means is formed, and alternately disposing the conversion means of the respective picture elements above and below to raise the photosensitivity.
CONSTITUTION: Sources 32 of lower layer on a P-type Si substrate 31 and sources 32 of a P-type layer 38 of upper layer through an SiO(sub 2) film 37 are alternately disposed, the source 32 as a photoelectric converter of MOSFET for forming a certain picture element is disposed in the lower layer, the photoelectric converter (source 32) adjacent to the picture element is disposed in the upper layer, the adjacent photoelectric converter further adjacent thereto is disposed in the lower layer, the photoelectric converters are alternately disposed in the upper and lower layers to expand the occupying area of the photoelectric converters, thereby efficiently receiving the incident light. Signals are alternately obtained form the upper and lower photoelectric converters, read out and then corrected. The Si layer of the upper layer is obtained by recrystallizing the polysilicon by using a laser or by hydrogenating it. The incident light among the picture elements is shielded by the photoconversion means of upper layer to be photoelectrically converted to eliminate false signals due to the incident light among the picture elements (in a wiring region).

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2/3,AB/9 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

01906366
SEMICONDUCTOR LIGHT DETECTING ELEMENT

PUB. NO.: 61-120466 [**JP 61120466** A]
PUBLISHED: June 07, 1986 (19860607)
INVENTOR(s): NAKANO MOTOO

APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-241978 [JP 84241978]
FILED: November 16, 1984 (19841116)
JOURNAL: Section: E, Section No. 446, Vol. 10, No. 306, Pg. 96, October 17, 1986 (19861017)

ABSTRACT

PURPOSE: To obtain an element, whose sensitivity to weak light is high, by forming the gate electrode of an IGFET having on conducting type channel by a reverse conducting type single crystal semiconductor, extending the electrode,, providing a one conducting type region at the extended part, forming a P-N junction by these parts, and using the element for detecting projected light.
CONSTITUTION: A thick element isolating film 12 is provided on the peripheral part of a P type Si substrate 11. An N(sup +) type drain region 15 and an N(sup +) type source region 16 are diffused and formed on the surface layer part of the sub strate 11 surrounded by the film 12. A thin gate oxide film 13 is deposited on the regions. A gate electrode 14 comprising a P(sup +) crystal is provided at the central part between the regions 15 and 16. Then, an N(sup +) type single crystal region 17 is diffused and formed on the surface layer part of the substrate 11 at the positions separated from the regions 15 and 16. The electrode 14 is extended on the region 17. A light receiving part 18 having a P-N junction J is formed. In this constitution, the sensitivity of the light detecting element to weak light is increased, signal leakage to other elements is eliminated and an after image time becomes short.

2/3,AB/10 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

01566556
PHOTO DETECTOR

PUB. NO.: 60-045056 [**JP 60045056** A]
PUBLISHED: March 11, 1985 (19850311)
INVENTOR(s): TSUBOUCHI NATSUO
YUYA NAOKI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-153536 [JP 83153536]
FILED: August 22, 1983 (19830822)
JOURNAL: Section: E, Section No. 329, Vol. 09, No. 173, Pg. 37, July 18, 1985 (19850718)

ABSTRACT

PURPOSE: To enable to generate high photocurrent with faint light and a small photo receiving area by optical exposure of part of the first impurity region.

CONSTITUTION: The light L of the invisible region generates holes and electrons in silicon. The electrons generated in a photo irradiated region 16 by irradiation of the optically exposed region 16 of the first impurity region 12 with the light L are collected to the plus charged second impurity region 13, and the holes flow to a semiconductor substrate 11. The holes flowing into this substrate 11 are amplified, and the inflow of electrons generates from the substrate 11 to the impurity region 12 and is further collected to the impurity region 13. The charges of the region 13

are rapidly discharged, and the discharged charges are charged from the third impurity region 14 by application of readout pulses on a gate electrode 15 at the time of readout of this photo charge. Then, this charged charge is observed as the photo signal.

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4/3,AB/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005  Thomson Derwent. All rts. reserv.

012588563
WPI Acc No: 1999-394670/199933
Related WPI Acc No: 1998-250435
XRAM Acc No: C99-115940
XRPX Acc No: N99-294992
  P-type intrinsic N-type photodiode for a photosensor
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: LIN C H
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No     Kind   Date     Applicat No     Kind   Date     Week
US 5920091     A   19990706  US 95542696      A   19951013  199933  B
                             US 9815448       A   19980129

Priority Applications (No Type Date): US 95542696 A 19951013; US 9815448 A
  19980129
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 5920091    A       5 H01L-029/04   Div ex application US 95542696
                                      Div ex patent US 5739065
Abstract (Basic): US 5920091 A
Abstract (Basic):
        NOVELTY - Structure comprises a semiconductor substrate with a
    p-type polysilicon layer on a gate oxide, separating source/drain
    regions (41). An intrinsic amorphous silicon layer on the P-type
    polysilicon layer and an N-type amorphous silicon layer on the
    intrinsic amorphous silicon layer form a gate. An indium tin oxide
    transparent conducting layer is on the N-type amorphous silicon layer.
    Silicon dioxide or nitride gate sidewall spacers (51) are beside the
    gate, adjacent the source/drain. Electrodes are formed on the gate and
    source/drain.
        USE - P-type intrinsic N-type (PIN) photodiode, for a photosensor,
    allocated in a MOSFET.
        ADVANTAGE - The photocurrent detected from the PIN photodiode is
    increased, thus a further amplifier circuit is not required.
        DESCRIPTION OF DRAWING(S) - The figure shows the photosensor.
        heavily doped region (41)
        gate sidewall spacers (51)
        pp; 5 DwgNo 6/6
```

6/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011528348
WPI Acc No: 1997-504829/**199747**
XRAM Acc No: C97-160804
XRPX Acc No: N97-420460

Flash memory with high programming and erasure efficiency - has thick hot electron injection layer for improved memory cell reliability

Patent Assignee: LG SEMICON CO LTD (GLDS ); GOLDSTAR ELECTRON CO LTD (GLDS ); HYUNDAI MICROELECTRONICS CO LTD (HYUN-N)
Inventor: LIM M G; PARK E J; LIM M; PARK E; PARK E C
Number of Countries: 004 Number of Patents: 007
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| DE 19648285 | A1 | 19971016 | DE 1048285 | A | 19961121 | 199747 | B |
| JP 9283644 | A | 19971031 | JP 96297950 | A | 19961022 | 199803 | |
| KR 97072450 | A | 19971107 | KR 9611064 | A | 19960412 | 199846 | |
| US 5841161 | A | 19981124 | US 97807979 | A | 19970303 | 199903 | |
| US 6124170 | A | 20000926 | US 97807979 | A | 19970303 | 200051 | |
| | | | US 9817926 | A | 19980203 | | |
| KR 192546 | B1 | 19990615 | KR 9611064 | A | 19960412 | 200056 | |
| DE 19648285 | C2 | 20001221 | DE 1048285 | A | 19961121 | 200101 | |

Priority Applications (No Type Date): KR 9611064 A 19960412
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| DE 19648285 | A1 | | 10 | H01L-027/115 | |
| JP 9283644 | A | | 6 | H01L-021/8247 | |
| KR 97072450 | A | | | H01L-027/115 | |
| US 5841161 | A | | | H01L-029/788 | |
| US 6124170 | A | | | H01L-021/8247 | Div ex application US 97807979 |
| KR 192546 | B1 | | | H01L-027/115 | |
| DE 19648285 | C2 | | | H01L-027/115 | |

Abstract (Basic): DE 19648285 A

The flash memory has: (a) a second conductivity type, preferably p-conducting, substrate (21) with spaced-apart first and second first conductivity type, preferably n-conducting, impurity **regions** (30,31), preferably source and drain regions; (b) a second conductivity type floating gate (25) above part of the first impurity region (30); (c) a first conductivity type floating gate (23a) above the second conductivity type floating gate (25); and (d) an insulation layer (28) and a control gate (29a) formed successively on the first conductivity type floating gate (23a).

Also claimed is flash memory production comprising: (i) successively forming a first insulating layer (22) and a first conductivity type first semiconductor layer on a substrate (21) except for a portion in which an erasing operation occurs; (ii) successively forming a second insulating layer (24) and a second conductivity type second semiconductor layer (25) on the erasing region; (iii) forming a first conductivity type third semiconductor layer on the first and second semiconductor layers; (iv) successively forming a third insulating layer (28) and a fourth semiconductor layer (29a) on the third semiconductor layer to cover at least part of the first and second semiconductor layers; (v) positioning a mask above the fourth semiconductor layer (29a) and selectively removing the first, second and third semiconductor layers to expose part of the substrate (21); and (vi) ion implanting first conductivity type impurities in the exposed substrate region to form impurity diffusion regions (30, 31).

ADVANTAGE - The flash memory has improved programming and erasure efficiency, provides increased programming and erasure power even at low voltage and provides improved memory cell reliability.

Dwg.4F/5

6/3,AB/2     (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010927715
WPI Acc No: 1996-424666/**199642**
Related WPI Acc No: 1998-144895
XRAM Acc No: C96-133785
XRPX Acc No: N96-357601

Formation of **p-n** junction floating gate ROM for multi-state memory devices - comprises forming a doped source and drain in a lightly doped P- semiconductor substrate, forming a tunnel oxide layer, etc. improving charge control erase efficiency

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N); TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: JIH G; CHI K M
Number of Countries: 002  Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5554552 | A | 19960910 | US 95415420 | A | 19950403 | 199642 | B |
| TW 288209 | A | 19961011 | TW 96101926 | A | 19960215 | 199708 | N |

Priority Applications (No Type Date): US 95415420 A 19950403; TW 96101926 A 19960215
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5554552 | A | | 23 | H01L-021/8247 | |
| TW 288209 | A | | | H01L-027/115 | |

Abstract (Basic): US 5554552 A

A method of forming a floating gate ROM device comprises (i) forming a doped source and drain in a lightly doped P-semiconductor substrate (11), (ii) forming a tunnel oxide layer (12) and field oxide region (43) and (iii) forming a PN junction floating gate electrode from a poly-Si layer comprising doped poly-Si with an **N**-doped **region** above the tunnel oxide and a **P**-doped **region** above the field oxide. An integrate electrode dielectric layer is formed over the floating gate electrode followed by a poly-Si control gate electrode and an additional dielectric layer.

Also claimed is a method as above in which an interpoly ONO dielectric layer is formed over the floating gate electrode followed by a control gate electrode, an additional dielectric layer having a via to the drain and a conductor extending through the via to contact the drain.

USE - Used for multi-state EEPROM and flash EPROM devices.

ADVANTAGE - The threshold voltage is well-controlled and erase efficiency and charge control are improved.

Dwg.1B/3

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 8/3,AB/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005  Thomson Derwent. All rts. reserv.

009833339
WPI Acc No: 1994-113195/199414
XRAM Acc No: C94-052197
XRPX Acc No: N94-088838
  Non-volatile semiconductor storage mfr. - comprising semiconductor
  substrate, impurity areas, impurity implanting layers, gate insulation
  film, floating gate electrode and control gate
  electrode
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ  )
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No     Kind   Date     Applicat No    Kind   Date     Week
JP 6061503     A   19940304  JP 92215151     A   19920812  199414  B

Priority Applications (No Type Date): JP 92215151 A 19920812
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
JP 6061503    A     15 H01L-029/788

Abstract (Basic): JP 6061503 A
        Compns. comprises: (A) an alkenyl gp.-contg. organopolysiloxane;
    (B) an organohydrogenpolysiloxane having at least 2 Si-bonded H atoms
    per mol.; (C) a Pt gp. metal catalyst; (D) an inorganic filler; (E) an
    organic Ti cpd.; and (F) water.
         The amt. of (B) provides 0.4-5.0 mols. Si-bonded H per mole
    alkenyl gps. in (A).
         USE/ADVANTAGE - The addn.-curable silicone rubber compsns. exhibit
    good fluidity and behave like a Newtonian fluids, even when inorganic
    fillers are incorporated to improve heat resistance, thermal
    conductivity, etc., and are useful as electrically-insulating potting
    compsns., PPC roll materials, etc.
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 8/3,AB/2     (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005  Thomson Derwent. All rts. reserv.

004635646
WPI Acc No: 1986-138989/198622
XRAM Acc No: C86-059409
XRPX Acc No: N86-102711
  Semiconductor photodetector device - comprises and IGFET with gate
  electrode and gate extension forming PN junction
Patent Assignee: FUJITSU LTD (FUIT  )
Inventor: NAKANO M
Number of Countries: 006  Number of Patents: 006
Patent Family:
Patent No     Kind   Date     Applicat No    Kind   Date     Week
EP 182610      A   19860528  EP 85308283     A   19851114  198622  B
JP 61120466    A   19860607  JP 84241978     A   19841116  198629
US 4841349     A   19890620  US 87113332     A   19871028  198931
EP 182610      B   19900117                                199003
DE 3575498     G   19900222                                199009
KR 8904476     B   19891104                                199043

Priority Applications (No Type Date): JP 84241978 A 19841116
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Patent Details:
Patent No  Kind Lan Pg  Main IPC  Filing Notes
EP 182610  A  E  18
Designated States (Regional): DE FR GB
EP 182610  B  E
Designated States (Regional): DE FR GB

Abstract (Basic): EP 182610 B

Photodetector comprises an IGFET having a channel of first type, **gate electrode** (14) of second type and gate extension (17) of first type. The **gate electrode** and **gate** extension form a pn junction (J) outside the channel region in an area (18) able to receive light.

**Gate electrode** and **gate** extension are pref. of doped Si, at least adjoining portions being mono-Si.

USE/ADVANTAGE - Used as an image element in a solid state imaging device. Photo-detector has good sensitivity and resolution and minimises lag or persistence. (18pp Dwg.No.1/4

Abstract (Equivalent): EP 182610 B

A semiconductor photodetector device comprising an insulating gate field effect transistor having a channel region of a first conductivity type, a **gate electrode** formed of a semiconductor of the same conductivity type, and a gate extension portion formed of a semiconductor of a second conductivity type, opposite to said first conductivity type, said **gate electrode** and said **gate** extension portion forming a photosensitive PN junction not located above the channel region of said transistor and an area including the PN junction being exposable to the incident light. (11pp)

Abstract (Equivalent): US 4841349 A

Semiconductor photodetector device, for a solid state image sensing device, comprises a) an insulating gate field effect transistor i) a channel region and source and drain regions of a first conductivity type, ii) a **gate electrode** of a 2nd conductivity type, opposite to the 1st conductivity type, and iii) a gate extension portion of the 1st conductivity type, ii) and iii), forming a PN junction outside i) and inside a photodetector area for detecting light; and b) means for applying a 1st voltage to iii) to reverse bias the PN junction and enable detection of light when the PN junction is conductive and supplies a voltage to ii), the voltage having a level determined by the intensity of the light of the photodetector area, and for applying a 2nd voltage to iii) to forward bias the PN junction, reset the photodetector device and release carriers stored in ii).

USE - Device serves as image element of a solid state imaging device. (9pp)e

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11/3,AB/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005  Thomson Derwent. All rts. reserv.

011200565
WPI Acc No: 1997-178490/199716
Related WPI Acc No: 1996-433087; 1998-446102; 2000-410860
XRPX Acc No: N97-147159
  Light responsive FET for semiconductor photodetector - has diode stack
  with variable number of planar junctions between gate and source to
  provide varying gate to source potential difference
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC  )
Inventor: LEAS J M; MANDELMAN J A
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No      Kind   Date     Applicat No     Kind   Date     Week
US 5610409      A   19970311  US 95371916       A   19950112  199716  B
                              US 96643675       A   19960506

Priority Applications (No Type Date): US 95371916 A 19950112; US 96643675 A
  19960506
Patent Details:
Patent No  Kind Lan Pg   Main IPC     Filing Notes
US 5610409    A      8 H01L-029/04   Cont of application US 95371916
                                     Cont of patent US 5557114

Abstract (Basic): US 5610409 A
        The FET has a gate with one or more light-responsive diodes stacked
    on the gate. Each diode has a planar e.g. horizontal
    junction. There is a source and a drain self-aligned to the diode.
    There is an electrical connection between the diode and the source.
        The number of diodes is chosen to achieve a desired gate to source
    potential difference. A channel region is between the source and drain,
    and it has a dielectric layer between itself and the gate.
        ADVANTAGE - Uses less space on chip. Few extra manufacturing steps
    over conventional FET. Customisable voltage output in response to
    light.
        Dwg.1/3
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14/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016228955
WPI Acc No: 2004-386844/**200436**
Related WPI Acc No: 2004-591637
XRAM Acc No: C04-144791
XRPX Acc No: N04-307797

Multi-bit flash memory for, e.g. personal computer, has isolation region that partitions floating gate into conductive blocks, and channel regions with different threshold voltages under the conductive blocks of different rows

Patent Assignee: MACRONIX INT CO LTD (MACR-N)
Inventor: CHANG K K
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6720613 | B1 | 20040413 | US 2003248374 | A | 20030115 | 200436 | B |

Priority Applications (No Type Date): US 2003248374 A 20030115
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 6720613 | B1 | | 12 | H01L-029/788 | |

Abstract (Basic): **US 6720613** B1
Abstract (Basic):

NOVELTY - Multi-bit flash memory comprises an isolation region that partitions a floating gate into conductive blocks to form multi-bit structure, and channel regions having different threshold voltages under the conductive blocks of different rows.

DETAILED DESCRIPTION - A multi-bit flash memory comprises a substrate (100), a control gate on the substrate, a floating gate (110) between the substrate and control gate, a gate dielectric layer (112) between the control gate and floating gate, a tunneling oxide layer (108) between the floating gate and substrate, a source region (104) and drain region (106) in the substrate at two sides of the floating gate, an isolation region (116) in the floating gate to partition the floating gate in conductive blocks arranged in an array with rows extending from the source region to the drain region and columns, and a channel region in the substrate under the floating gate between the source and drain regions. Before writing data into the multi-bit flash memory, the channel region under the conductive blocks of the same row has the same threshold voltage, and the channel region under the conductive blocks of a different row has different threshold voltages. Each row comprises two conductive blocks (110a-110d) and each column comprises n (a positive integer) conductive blocks.

USE - For personal computer and electronic equipment.

ADVANTAGE - Meets the high-density data storage requirement and can store multiple bits to increase device integration. The over-erase is avoided and the reliability of the flash memory is enhanced. The problem of secondary electron injection is resolved.

DESCRIPTION OF DRAWING(S) - The figures show a top view and a cross-sectional view of a multi-bit flash memory.

Substrate (100)
Source region (104)
Drain region (106)
Tunneling oxide layer (108)
Floating gate (110)
Conductive blocks (110a-110d)
Gate dielectric layer (112)

```
        Isolation region (116)
        pp; 12 DwgNo 1A, 1B/4


 14/3,AB/2     (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015863542
WPI Acc No: 2004-021373/200402
Related WPI Acc No: 2001-556779; 2002-082335
XRAM Acc No: C04-006799
XRPX Acc No: N04-016413
  Fabrication of tunnel photodiode used to form photosensitive device, by
  forming p-type semiconductor layer as bottom electrode, forming thin
  insulator layer on the bottom electrode, and depositing thin conducting
  layer as top electrode
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: JAN C; WANG J; WU L; YIU H
Number of Countries: 001  Number of Patents: 002
Patent Family:
Patent No       Kind   Date    Applicat No     Kind    Date     Week
US 20030203525   A1   20031030  US 2001904138    A   20010713  200402  B
                                US 2003437147    A   20030513
US 6693317      B2   20040217  US 2001904138    A   20010713  200413
                                US 2003437147    A   20030513

Priority Applications (No Type Date): US 2001904138 A 20010713; US
  2003437147 A 20030513
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 20030203525 A1     6 H01L-021/00   Div ex application US 2001904138
                                     Div ex patent US 6582981
US 6693317    B2       H01L-029/76   Div ex application US 2001904138
                                     Div ex patent US 6582981

Abstract (Basic): US 20030203525 A1
Abstract (Basic):
        NOVELTY - A tunnel photodiode is fabricated by providing a
    substrate (8) and forming a p-type semiconductor layer on the substrate
    to be the bottom electrode; forming a thin insulator layer (10) on the
    bottom electrode; and depositing a thin conducting layer to be top
    electrode.
        USE - The method is for fabricating a tunnel photodiode.
        ADVANTAGE - The tunnel photodiode provides photosensitive device
    having minimal dark current such that the ratio of current in light to
    dark current increases with increasing bias, thus at even low light
    intensities the photo-induced current can be made to exceed the dark
    current.
        DESCRIPTION OF DRAWING(S) - The figure shows a tunnel photodiode.
        P-well (2)
        N-type polysilicon (4)
        Ammeter (6)
        Substrate (8)
        Insulator layer (10)
        pp; 6 DwgNo 3/6


 14/3,AB/3     (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015062451
WPI Acc No: 2003-122967/**200312**
XRAM Acc No: C03-031976
XRPX Acc No: N03-097920

Semiconductor device with a Dynamic Random Access Memory type integrated memory based on the confinement of a negative or positive charge in one or other of two potential wells

Patent Assignee: STMICROELECTRONICS SA (SGSA )
Inventor: SCOTNICKI T; VILLARET A; SKOINICKI T; SKOTNICKI T
Number of Countries: 028 Number of Patents: 005

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| FR 2826180 | A1 | 20021220 | FR 20018051 | A | 20010619 | 200312 | B |
| EP 1271657 | A1 | 20030102 | EP 2002291390 | A | 20020606 | 200312 | |
| US 20030006431 | A1 | 20030109 | US 2002174490 | A | 20020618 | 200312 | |
| JP 2003060095 | A | 20030228 | JP 2002178046 | A | 20020619 | 200325 | |
| US 6759721 | B2 | 20040706 | US 2002174490 | A | 20020618 | 200444 | |

Priority Applications (No Type Date): FR 20018051 A 20010619

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| FR 2826180 | A1 | | 44 | H01L-021/8239 | |
| EP 1271657 | A1 | F | | H01L-029/788 | |

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20030006431 | A1 | | | H01L-031/72 | |
| JP 2003060095 | A | | 13 | H01L-021/8247 | |
| US 6759721 | B2 | | | H01L-027/14 | |

Abstract (Basic): **FR 2826180** A1

Abstract (Basic):

NOVELTY - An integrated memory semiconductor device comprises:

(a) an integrated structure of point memory incorporating a semiconductor layer covered with an insulating envelope (CH2), between the source (S) and drain (D) regions of a transistor and interpolated between its canal region and control grid and including two potential well zones (Z1, Z3) separated by a potential barrier zone (Z2) under the control grid (GC);

(b) a writing system (Vg, Vds) able to polarise the structure of point memory to confine some charge carriers selectively in one or other of the potential well zones;

(c) a reading system (Vg, Vd) able to polarize the structure of point memory to detect the presence of the charge carriers in one of the potential wells.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) an integrated circuit incorporating at least one of these semiconductor devices;

(b) a method for the fabrication of such a semiconductor device.

USE - The integrated memory semiconductor device is for use in integrated circuits for memory semiconductors.

ADVANTAGE - The invention provides an integrated memory semiconductor device offering hybrid performances of classical Flash and DRAM cells, whilst freeing itself of their respective limitations. It uses a point memory that has the compactness of a single transistor. It allows access times of some nanoseconds and is much more rapid then the tunnel effect used in flash technology.

DESCRIPTION OF DRAWING(S) - The drawings illustrate two modes of realization of a memory device.

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        pp; 44 DwgNo 12/24


 14/3,AB/4     (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012353448
WPI Acc No: 1999-159555/199914
XRPX Acc No: N99-116152
  Non-volatile semiconductor memory e.g. EEPROM - includes source and drain
  formed on such that floating gates which are formed on substrate at
  different areas are arranged parallelly
Patent Assignee: NEC CORP (NIDE  ); NIPPON ELECTRIC CO (NIDE  )
Inventor: KAWATA M
Number of Countries: 003  Number of Patents: 005
Patent Family:
Patent No     Kind   Date    Applicat No    Kind   Date     Week
JP 11017037    A   19990122  JP 97171687     A   19970627  199914  B
US 5999453     A   19991207  US 98104953     A   19980625  200004
KR 99007378    A   19990125  KR 9824364      A   19980626  200014
JP 3070531     B2  20000731  JP 97171687     A   19970627  200041
KR 346021      B   20020918  KR 9824364      A   19980626  200317

Priority Applications (No Type Date): JP 97171687 A 19970627
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
JP 11017037   A     12 H01L-021/8247
US 5999453    A        G11C-016/04
KR 99007378   A        H01L-027/115
JP 3070531    B2    12 H01L-021/8247 Previous Publ. patent JP 11017037
KR 346021     B        H01L-027/115  Previous Publ. patent KR 99007378

Abstract (Basic): JP 11017037 A
        NOVELTY - Floating gates (103a,103b) which consists of
    polycrystalline silicon are formed on a semiconductor substrate (101)
    at different areas, via a gate insulating film (102). Control gates
    (105a,105b) made of polycrystalline Si are formed on the respective
    floating gates via an insulated separation membrane (104), source (106)
    and drain (107) are formed on the semiconductor substrate such that the
    floating gates are arranged parallelly.
        USE - EEPROM.
        ADVANTAGE - Suppresses increase in number of memory cells and
    channel resistance. Loading of memory peripheral circuit is prevented.
    By sharing source between adjacent memory cells, degree of integration
    is improved. DESCRIPTION OF DRAWING(S) - The figure shows schematic
    plan and sectional view of the components of non volatile semiconductor
    memory. (101) Semiconductor substrate; (102) Gate insulating film;
    (103a,103b) Floating gates; (104) Insulated separation member;
    (105a,105b) Control gates; (106) Source; (107) Drain.
        Dwg.1/8


 14/3,AB/5     (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012202677
WPI Acc No: 1999-008783/199901
XRAM Acc No: C99-003043
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New dihydro-benzo(b)indeno(2,1-d)thiophene derivatives - useful for inhibition of bone loss and resorption associated, lowering serum cholesterol and treatment of oestrogen dependent cancer

Patent Assignee: LILLY & CO ELI (ELIL ); WAFERSCALE INTEGRATION INC (WAFE-N)

Inventor: BELL M G; MUEHL B S; WINTER M A; KAZEROUNIAN R

Number of Countries: 001 Number of Patents: 002

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5834488 | A | 19981110 | US 9626718 | A | 19960926 | 199901 | B |
| | | | US 97933414 | A | 19970919 | | |
| US 5949711 | A | 19990907 | US 9626718 | A | 19960926 | 199943 | |
| | | | US 97936849 | A | 19970924 | | |

Priority Applications (No Type Date): US 9626718 P 19960926; US 97933414 A 19970919; US 97936849 A 19970924

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 5834488 | A | | 27 | A61K-031/445 | Provisional application US 9626718 |
| US 5949711 | A | | | G11C-016/04 | Provisional application US 9626718 |

Abstract (Basic): US 5834488 A

Dihydrobenzo[b]indeno[2,1-d]thiophene derivatives of formula (I), their salts and solvates are new. R1-R4 = H, OH, halo, O(1-4C alkyl), OCO(1-6C alkyl), OCO(O)(1-6C alkyl), OCOAr1, OCO(O)Ar1 or OSO2(4-6C alkyl); Ar1 = optionally substituted phenyl; Q = (CH2)2R5 or (CH2)3R5; R5 = 1-piperidinyl, 1-pyrrolidinyl, methyl-1-pyrrolidinyl, dimethyl-1-pyrrolidinyl, 4-morpholino, dimethylamino, diethylamino or 1-hexamethylene-imino; R6 = H, OH, halogen, CN, NH2, NHR7 or NR7R8; and R7, R8 = 1-6C alkyl.

USE - (I) are useful for inhibiting bone loss or resorption, particularly due to menopause or ovariectomy, for lowering serum cholesterol levels and inhibiting oestrogen-dependent cancer, particularly breast or uterine cancer (claimed), for treatment of osteoporosis and cardiovascular conditions e.g. hyperlipidaemia.

ADVANTAGE - (I) have reduced side-effects compared with oestrogen therapy.

Dwg.0/0

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14/3,AB/6 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011894645

WPI Acc No: 1998-311555/**199827**

XRAM Acc No: C98-096081

XRPX Acc No: N98-244207

Forming a barrier layer for use in integrated circuit structures - comprising of amorphous zirconium titanium oxide around conventional and perovskite ferroelectric dielectrics

Patent Assignee: NORTHERN TELECOM LTD (NELE )

Inventor: CHIVUKULA V; LEUNG P K

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 5753945 | A | 19980519 | US 95658 | A | 19950629 | 199827 | B |
| | | | US 96595116 | A | 19960201 | | |

Priority Applications (No Type Date): US 95658 P 19950629; US 96595116 A

```
  19960201
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 5753945    A      6 H01L-029/76   Provisional application US 95658
Abstract (Basic): US 5753945 A
        An integrated circuit structure has a dielectric barrier layer (44)
    between a perovskite ferroelectric layer (36) and another material
    (42). The barrier layer is zirconium titanium oxide, as ZrTiO4.
        USE - Preparing a barrier layer for use in integrated circuit
    structures, especially in ferroelectric memory elements, and
    ferroelectric capacitors.
        ADVANTAGE - The barrier layer is compatible with conventional and
    perovskite ferroelectric materials. It is processed at 8000C, which is
    compatible with integrated circuit processing.
        Dwg.3/3


 14/3,AB/7     (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011499529
WPI Acc No: 1997-477442/199744
XRPX Acc No: N97-398226
  Non-volatile memory - has program gate provided in upper part of each
  second floating gate which covers upper part of density layer
Patent Assignee: NIPPON MOTOROLA KK (MOTI  ); MOTOROLA INC (MOTI  )
Inventor: KOJIMA T
Number of Countries: 002  Number of Patents: 003
Patent Family:
Patent No      Kind   Date     Applicat No     Kind   Date      Week
JP 9223753      A   19970826  JP 9630779        A   19960219  199744  B
US 5789777      A   19980804  US 97778410       A   19970102  199838
JP 3001409      B2  20000124  JP 9630779        A   19960219  200009

Priority Applications (No Type Date): JP 9630779 A 19960219
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
JP 9223753    A     16 H01L-021/8247
JP 3001409    B2    15 H01L-021/8247 Previous Publ. patent JP 9223753
US 5789777    A        H01L-029/76
Abstract (Basic): JP 9223753 A
        The memory has a memory cell which has a semiconductor substrate. A
    source (2) and a drain (3) are formed in the substrate separately. A
    first floating gate (4A) is distributed between the source and drain in
    the upper part of the substrate. A control gate (5) is distributed
    between the source and drain in the upper part of first floating gate.
        A pair of high impurity layers (21,22) are formed on the substrate,
    separated from the drain and source. A set of second floating gates
    (4B1,4B2) are set up covering the upper part of each density layer,
    crossing the first floating gate. A set of program gates (61,62) is
    distributed in the upper part of each floating gate.
        ADVANTAGE - Increases memory capacity. Reduces power consumption.
    Increases life.
        Dwg.9/24


 14/3,AB/8     (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010936137
WPI Acc No: 1996-433087/199643
Related WPI Acc No: 1997-178490; 1998-446102; 2000-410860
XRPX Acc No: N96-364938
  Light-responsive FET for e.g. semiconductor image sensor - has two
  vertically stacked light responsive diodes adjacent gate and separated
  from each other by titanium nitride ohmic contact
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC  ); IBM CORP (IBMC  )
Inventor: LEAS J M; MANDELMAN J A
Number of Countries: 003  Number of Patents: 003
Patent Family:
Patent No     Kind   Date     Applicat No    Kind   Date      Week
US 5557114     A   19960917  US 95371916      A   19950112  199643  B
TW 295719      A   19970111  TW 95108332      A   19950810  199717
KR 222220      B1  19991001  KR 9550393       A   19951215  200108

Priority Applications (No Type Date): US 95371916 A 19950112
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 5557114    A      7 H01L-031/062
TW 295719     A        H01L-027/105
KR 222220     B1       H01L-029/739

Abstract (Basic): US 5557114 A
        The FET (40) includes a gate (22) and at least two stacked light
    responsive diodes (24,42) vertically adjacent the gate. Each of the two
    stacked diodes including a planar junction. Also provided is an ohmic
    contact (52), e.g. titanium nitride, between each of the stacked
    diodes.
        USE/ADVANTAGE - For charge storage in solid-state image sensor.
    Minimises use of FET area and number of processing steps. Provides
    customisable in response to light.
        Dwg.2/3


 14/3,AB/9     (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010277153
WPI Acc No: 1995-178408/199523
XRPX Acc No: N95-140123
  Programming method for floating gate memory cell using single low voltage
  supply - pumping source of selected cell to voltage less than supply
  level VSS at reference-voltage terminal of array, and simultaneously
  pumping drain of cell to greater than VCC
Patent Assignee: TEXAS INSTR INC (TEXI  )
Inventor: KAYA C; SCHRECK J F; MCELROY D J
Number of Countries: 007  Number of Patents: 005
Patent Family:
Patent No     Kind   Date     Applicat No    Kind   Date      Week
US 5412603     A   19950502  US 94239008      A   19940506  199523  B
EP 681296      A2  19951108  EP 95106827      A   19950505  199549
JP 8045291     A   19960216  JP 95108792      A   19950502  199617
EP 681296      B1  20010919  EP 95106827      A   19950505  200155
DE 69522738    E   20011025  DE 622738        A   19950505  200171
                             EP 95106827      A   19950505

Priority Applications (No Type Date): US 94239008 A 19940506
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Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 5412603    A      10 G11C-007/00
EP 681296     A2 E   12 G11C-016/06
   Designated States (Regional): DE FR GB IT NL
JP 8045291    A      10 G11C-016/06
EP 681296     B1 E      G11C-016/06
   Designated States (Regional): DE FR GB IT NL
DE 69522738   E         G11C-016/06   Based on patent EP 681296

Abstract (Basic): US 5412603 A
        The method for programming a floating-gate memory cell in a
    nonvolatile integrated-circuit memory having a reference-voltage
    terminal and a supply-voltage terminal, involves applying a first
    voltage to the source of the memory cell, and which is less than the
    voltage at the reference-voltage terminal. A second voltage is applied
    to the drain of the memory cell, and is greater than the voltage at the
    supply-voltage terminal.
        A third voltage is applied to the control gate, the third voltage
    greater than the voltage at the reference-voltage terminal. The memory
    cell is formed in and on a semiconductor isolation well, and a fourth
    voltage is applied to the semiconductor isolation well, and is less
    that the first voltage.
        USE/ADVANTAGE - E.g. floating gate memory array. Programs selected
    nonvolatile cell by hot carrier injection. Efficiently uses charge pump
    circuit to raise selected cell to desired voltage.
        Dwg.1/9


 14/3,AB/10     (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009370089
WPI Acc No: 1993-063568/199308
XRPX Acc No: N93-048431
  Photoelectric converter for facsimile machines and image readers -
  prevents deformation of upper electrode layer by stabilising each layer
  thickness, minimising leakage current  NoAbstract
Patent Assignee: CANON KK (CANO  )
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No     Kind   Date     Applicat No    Kind   Date     Week
JP 5013803     A   19930122  JP 91184164     A   19910628  199308  B

Priority Applications (No Type Date): JP 91184164 A 19910628
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
JP 5013803    A       8 H01L-031/10

Abstract (Basic): JP 5013803 A
        Dwg.4/12


 14/3,AB/11     (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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008544294
WPI Acc No: 1991-048357/199107
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XRPX Acc No: N91-037364
Flat cable for power supply to elevator cage - has parallel stranded reinforcing wires in cable sheath and along cable length NoAbstract Dwg 4-6/6
Patent Assignee: FUJIKURA LTD (FUJD )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 3001409 | A | 19910108 | JP 89134574 | A | 19890530 | 199107 | B |

Priority Applications (No Type Date): JP 89134574 A 19890530

14/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004269637
WPI Acc No: 1985-096515/**198516**
Light detector - has high sensitivity even if light is weak or surface admitting light in small NoAbstract Dwg 3/3
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 60045056 | A | 19850311 | JP 83153536 | A | 19830822 | 198516 | B |

Priority Applications (No Type Date): JP 83153536 A 19830822
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 60045056 | A | | 5 | | |

14/3,AB/13 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

07658261
MEMORY DEVICE AND INTEGRATED CIRCUIT

| | |
|---|---|
| PUB. NO.: | 2003-152119 [**JP 2003152119** A] |
| PUBLISHED: | May 23, 2003 (20030523) |
| INVENTOR(s): | DRAY CYRILLE<br>CASPAR DANIEL<br>FOURNEL RICHARD |
| APPLICANT(s): | ST MICROELECTRONICS SA |
| APPL. NO.: | 2002-252983 [JP 2002252983] |
| FILED: | August 30, 2002 (20020830) |
| PRIORITY: | 01 200111381 [FR 200111381], FR (France), September 03, 2001 (20010903) |

ABSTRACT

PROBLEM TO BE SOLVED: To provide an FAMOS memory location which can have at least three completely natural program levels.

SOLUTION: An FAMOS memory location is provided with a single floating gate (GR) overlapping the active plane of a semiconductor substrate along contour (PF1, PF2) of at least two asymmetric overlaps in order to determine at least two electrodes in an active region. A memory location

program means (MC, SW) applies a set of specified different voltages selectively to the electrodes such that at least three program logical levels are outputted to the memory location.

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14/3,AB/14 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

05668844
STRUCTURE AND MANUFACTURE OF FLASH MEMORY

PUB. NO.: 09-283644 [**JP 9283644** A]
PUBLISHED: October 31, 1997 (19971031)
INVENTOR(s): MIN KIYU IMU
UN ZON PAKU
APPLICANT(s): L JII SEMICON CO LTD [000000] (A Non-Japanese Company or Corporation), KR (Korea) Republic of
APPL. NO.: 08-297950 [JP 96297950]
FILED: October 22, 1996 (19961022)
PRIORITY: 9611064 [KR 9611064], KR (Korea) Republic of, April 12, 1996 (19960412)

14/3,AB/15 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO

05515037
SEMICONDUCTOR MEMORY DEVICE AND ITS PREPARATION

PUB. NO.: 09-129837 [**JP 9129837** A]
PUBLISHED: May 16, 1997 (19970516)
INVENTOR(s): GUN HIYON BAKU
APPLICANT(s): L G SEMICON CO LTD [000000] (A Non-Japanese Company or Corporation), KR (Korea) Republic of
APPL. NO.: 08-281285 [JP 96281285]
FILED: October 03, 1996 (19961003)
PRIORITY: 9534120 [KR 9534120], KR (Korea) Republic of, October 05, 1995 (19951005)